APPLICATION NOTE

The TDA8376/TDA8376A demonstration board PR32031

AN96035

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Abstract

The PR32031 demo board is made to demonstrate the alignment-free I²C-bus controlled TDA8376(A), which contains a PAL/NTSC colour decoder, luminance processor, sync processor, RGB controller and deflection processor.

The demo board contains the baseband delay line TDA4665, the alignment free SECAM decoder TDA8395 and the TDA8350 DC coupled vertical deflection output circuit with East-West output circuit. External CVBS, RGB and S-VHS signals can be processed.

Purchase of Philips I²C components conveys a license under the I²C patent to use the components in the I²C system, provided the system conforms to the I²C specifications defined by Philips.

APPLICATION NOTE

The TDA8376(A) demonstration board PR32031

AN96035

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Summary

This report describes the demonstration board, built around the single chip I²C bus controlled PAL/NTSC TV-processors TDA8376(A):

- Chapter 1 is a guide to get your TDA8376(A) demonstration board working.
- Chapter 2 gives a short feature overview of the TDA8376(A) one-chip device (for detailed and up-to-date information, please consult the data sheet, ref. [1]). Further it shows the interfacing of YUV-based features like the TDA9170 Picture Booster and Y/C based TDA4961 comb filter.
- Chapter 3 describes the applied circuits and the physical layout of the demonstration board.

The TDA8376(A) combines the synchronization, video and deflection functions for a colour television. It includes switches for CVBS, S-VHS and RGB. All functions are controlled by I²C bus. Also relevant status information can be read via this bus. On the TDA8376(A) demo board the TDA4665 delay line, the TDA8395 alignment free SECAM decoder and a TDA8350 DC coupled vertical deflection circuit with East West amplifier are used.

The TDA8376(A) is equipped with Vertical geometry and East-West control for 110° picture tube applications. It has been designed to be used in combination with the TDA8350, TDA8351 or TDA8356 family of vertical output stages. For 16:9 applications the TDA8376 has some vertical zoom possibilities, the TDA8376A has as additional feature flexible horizontal and vertical zoom possibilities.

On the demo board a connector is available for plug-in YUV features.

By plugging in a small horizontal-flyback simulator panel, the sync behaviour of the TDA8376(A) can be tested with variable flyback pulse position and width, without connecting a horizontal deflection circuit. Alternatively, the PR32031 demonstration board can be connected to a Power & Deflection board (PR31082), a CRT panel (PR32051) and a picture tube, to make it a real monitor.

The TDA8376(A) demonstration board is controlled via I²C-bus by an ”ICP” menu, running from a personal computer. The menu shows all internal functions of the TDA8376(A).

The TDA8376/TDA8376A demonstration board PR32031

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FIGURES

TABLES

ABBREVIATIONS

BTL	**B**ridge **T**ied **L**oad, the load is connected between two differential outputs
EMC	**E**lectro **M**agnetic **C**ompatibility
IC	**I**ntegrated **C**ircuit
ICP	**I²C**-bus **C**ontrol **P**rogram, family of Personal Computer-based software tools
EHT	**E**xtra **H**igh **T**ension, 27.5kV anode voltage of the picture tube.
LOT	**L**ine **O**utput **T**ransformer, delivers EHT, focus, V_{G2} voltage.
OSD	**O**n **S**creen **D**isplay
RGB	**R**ed, **G**reen, **B**lue colour signals.
YUV	Luminnance (**Y**) and colour difference signals (**U**,**V**)
a .. b	Indicates a range from ”a” to ”b”

1. Introducing the TDA8376(A) demonstration board.

The TDA8376(A) demonstration package consists of the following items:

- Floppy-disk ”ICP” program for personal computer.
- PR30921 Centronics to single master I²C-bus interface (or equivalent).
- PR32031 Small signal board for TDA8376(A).
- PR32031-01 H-flyback simulator.
- PR32031-02 Monitor output of RGB_{OUT} and $CVBS_{OUT}$ via Scart connector.

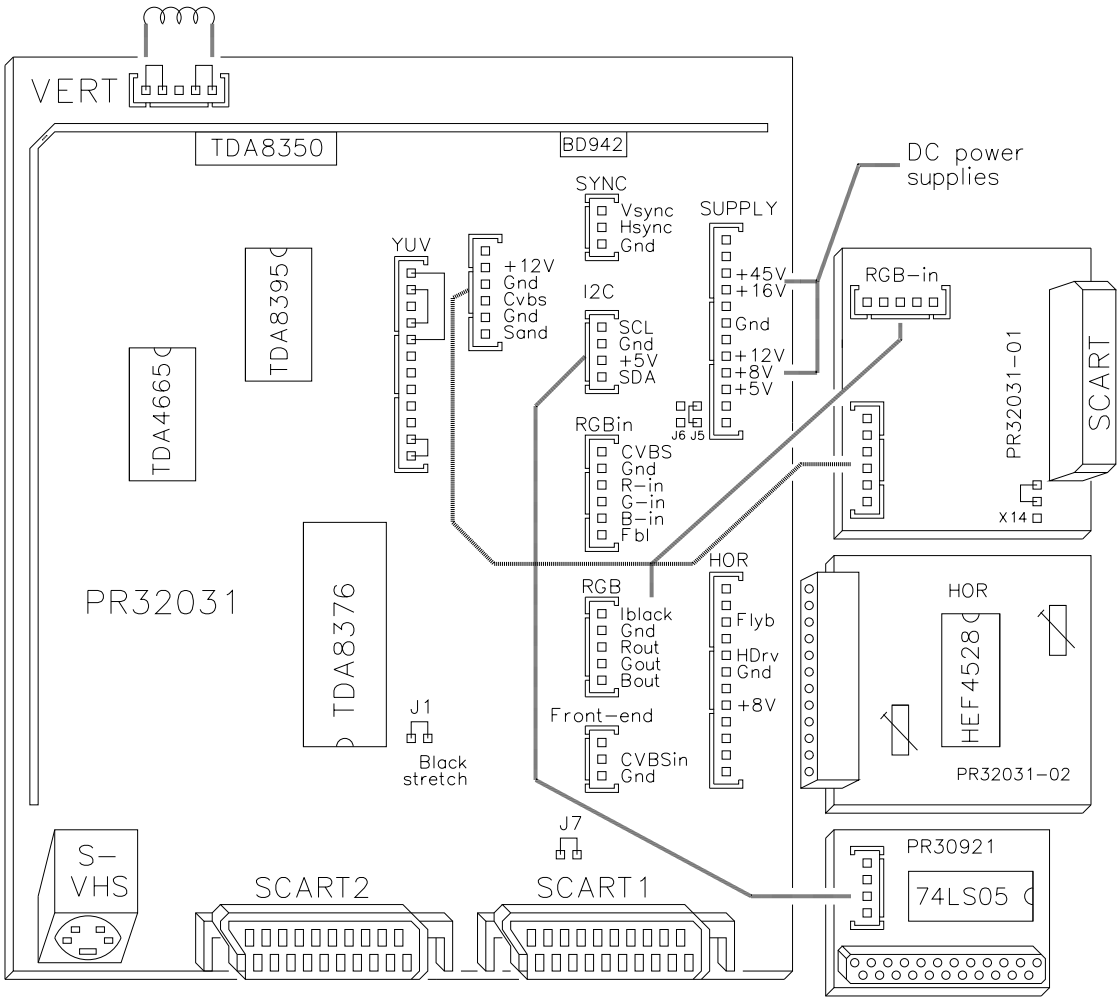


Figure 1 How to connect the demonstration board.

Note: When the vertical deflection coil is not connected, the vertical guard protection should be disabled (bit **EVG**, see chapter 2.10.7, page 26), otherwise the RGB_{OUT} outputs are blanked (protection against burn-in of the picture tube).

Connect the boards in the following way:

- Connect the PR32031-01 monitor panel with two 1:1 cables to plugs X4 ”RGB-out” and X13. Via a scart plug the signal processing of the TDA8376(A) can be checked on a monitor. The plug carries the following signals: output of the CVBS switch and the RGB outputs of the TDA8376(A). Jumper X14 can activate the RGB status pin on the monitor panel. The black-current loop is simulated through via a special circuit consisting of D7-12, T8,16,17, R61,62,66,68,69,75,76 (see Figure 11, Page 39).
- Plug the PR32031-02 H-flyback simulator panel in plug X9 ”HOR”. With the two potentiometers on the simulator board, a H-flyback pulse with variable position and width can be set.
- Insert a YUV dummy plug to connect $R\text{-}Y_{IN,OUT}$, $B\text{-}Y_{IN,OUT}$ and $Y_{IN,OUT}$.
- Connect the PR30921 single master I²C-bus interface via a 1:1 cable to plug X7 ”I2C”.
- Connect the interface to a Centronics (parallel) port of a personal computer. The two jumpers on the interface board must be closed. They connect pull-up resistors to SDA and SCL.
- Connect D.C. power supplies of +45 V, +16 V, (+12 V), +8 V and +5 V to plug X8 ”SUPPLY”.
- Put the ”ICP” floppy in the disk drive of the personal computer and type ”GO” to start the software. Now use the TDA8376(A) menu to control the PR32031 demonstration board. On-line help is available by pressing ”?”. For more information on ”ICP” menu’s see ref. [9]
- Open jumper ”J1” to enable the black stretch function of the TDA8376(A).
- Connect a vertical deflection coil to plug X6 ”Vert-Defl” or make sure that bit **EVG** (see chapter 2.10.7, page 26) is set.
- When you switch on the board for the very first time, some alignment may be necessary to get optimal performance (see chapter 4.2 on page 37).

When the scart monitor PR32031-01 and H-flyback simulator PR32031-02 are omitted, the package can be completed to drive 110° picture tubes by connecting a power supply board, which also contains the horizontal deflection. A separate CRT panel is available with the video output amplifiers. For more information, please contact your PHILIPS representative (see ref.[6]) about the availability of the following panels:

- PR32051 CRT panel with 3x TDA6101 RGB amplifiers (with black current output)
- PR31082 120 W power supply with 110° deflection, including East-West diode modulator

For application information on power supplies, see ref. [2] and [3].

Besides the TDA8376(A) single chip, the PR32031 demonstration board contains the following circuits (see also the block diagram of Figure 6 on page 27):

- Alignment free switch capacitor base band delay line TDA4665.
- Alignment free SECAM decoder TDA8395.
- DC coupled vertical deflection stage TDA8350 with East-West amplifier.
- YUV add-on option plug for YUV-based signal improvement circuits. When not used, a dummy plug should be inserted to connect $R\text{-}Y_{IN,OUT}$, $B\text{-}Y_{IN,OUT}$ and $Y_{IN,OUT}$.

2. Internal functions of the TDA8376(A).

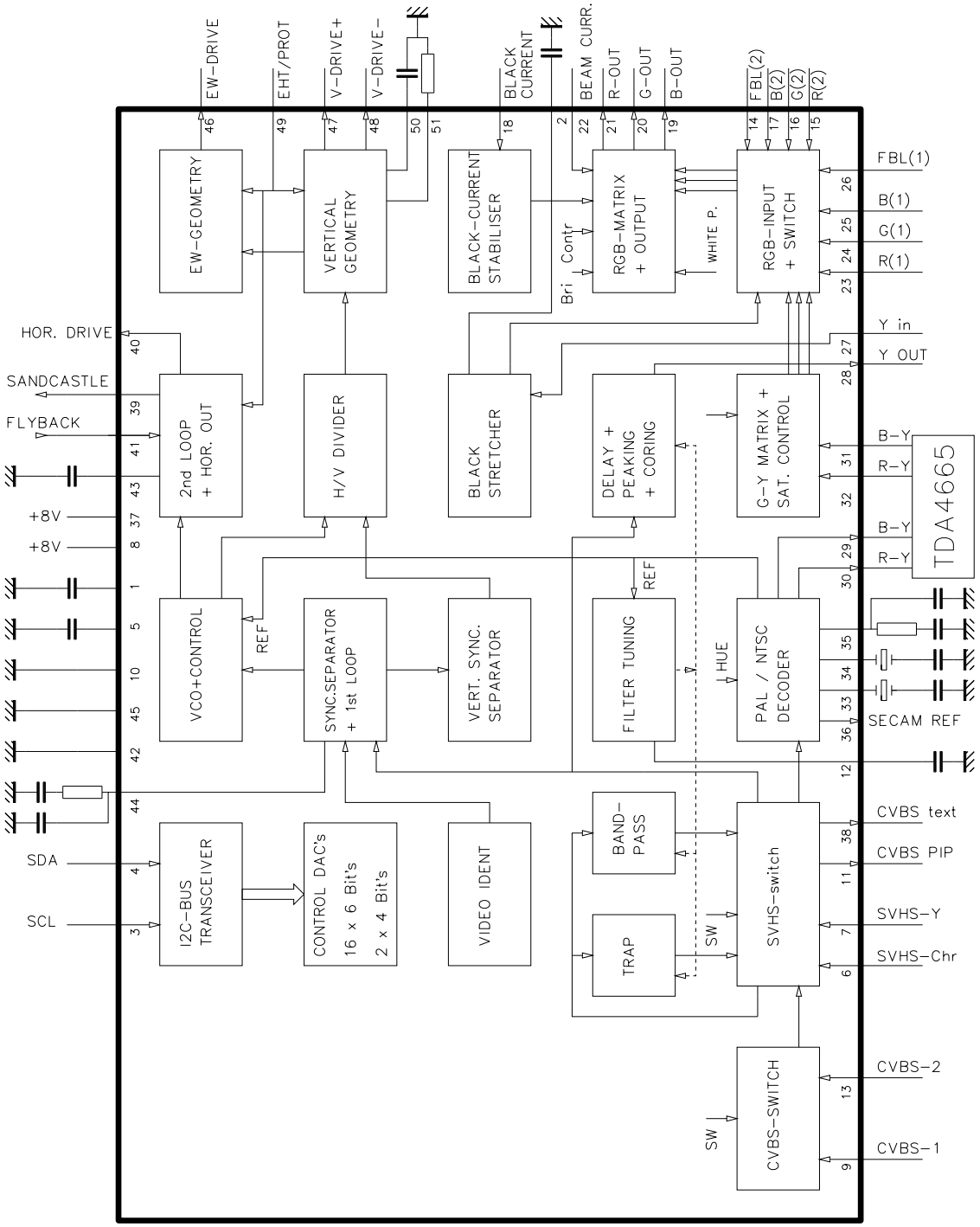


Figure 2 Internal block diagram of TDA8376(A).

2.1. Pinning.

The table below shows the pinning of the 52 pin S-DIL version of the TDA8376(A), because this version is used on the demo board. The TDA8376(A) is also defined as a QFP-64 package. The pinning of this device can be found in the device specification, ref.[1]. Engineering samples of the QFP-64 package can be obtained, see ref. [6]. The QFP-64 package is not yet in production. All pin numbers mentioned in the remaining of this document refer to the S-DIL package.

Pin	Function	Pin	Function
1	Decoupling digital supply	52	n.c.
2	Black peak hold capacitor	51	Vertical current reference
3	SCL (I^2C bus)	50	Vertical sawtooth capacitor
4	SDA (I^2C bus)	49	EHT/ Over-voltage protection$_{IN}$
5	Bandgap decoupling	48	Vertical I-drive+$_{OUT}$
6	Input C_{S-VHS}	47	Vertical I-drive-$_{OUT}$
7	Input Y_{S-VHS} (or $CVBS3_{EXT}$)	46	East-West drive$_{OUT}$
8	Main +8V supply	45	Ground
9	Input CVBS1	44	Phi 1-loop filter
10	Ground	43	Phi 2-loop filter
11	Output $CVBS_{pip}$	42	Ground
12	Decoupling filter tuning	41	H-flyback$_{IN}$
13	Input CVBS2	40	H_{OUT}
14	Fast blank RGB_2	39	Sandcastle$_{OUT}$
15	Input R_2	38	Output $CVBS_{TXT}$
16	Input G_2	37	+8V supply
17	Input B_2	36	SECAM chroma reference$_{OUT}$
18	Black current$_{IN}$	35	Colour PLL filter
19	B_{OUT}	34	X-tal 4.43/3.58 MHz
20	G_{OUT}	33	X-tal 3.58 MHz
21	R_{OUT}	32	R-Y_{IN}
22	Beam current limiter	31	B-Y_{IN}
23	Input R_1	30	R-Y_{OUT}
24	Input G_1	29	B-Y_{OUT}
25	Input B_1	28	Y_{OUT}
26	Fast Blank RGB_1	27	Y_{In}

Table 1. Pinning of TDA8376(A).

2.2. Source select switch.

Controlled by I²C bus, the TDA8376(A) input switch can select one of the following sources:

- pin 9 : CVBS1
- pin 13 : CVBS2
- pin 7 : CVBS3
- pin 7, pin 6 : $Y_{S\text{-}VHS}$, $C_{S\text{-}VHS}$

Both CVBS outputs can be chosen independently from each other, out of the inputs:

- pin 38 : $CVBS_{TXT}$
- pin 11 : $CVBS_{PIP}$

In case a Y/C signal is selected, the luminance and chroma is combined to a CVBS signal on the CVBS outputs. The signal selected for the internal colour decoder and sync circuit is also available at the $CVBS_{TXT}$ output. This implies that this signal can be used to drive teletext or the TDA8395 SECAM add-on.
For comb filter applications the $CVBS_{PIP}$ output can be connected to the input of the comb filter and thus the input signal of the comb filter can be selected. The outputs of the comb filter are connected to the Y/C inputs which are selected as input for the internal colour decoder (and output at the $CVBS_{TXT}$ output). Figure 4 shows how a comb filter can be used in combination with the TDA8376(A).
The $S\text{-}VHS_Y$ input can also be used as a CVBS(3) input. This mode can be selected with bit **CVS**.
There is also an automatic S-VHS mode available. In this mode the signal of CVBS2 (pin13) is processed, until sync pulses are detected on the $S\text{-}VHS_Y$ input, this state can be detected by reading the bit **STS**.

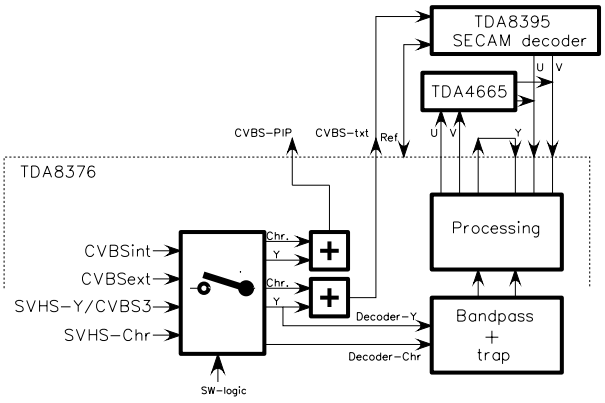


Figure 3 Source switch, delay line and SECAM decoder connection.

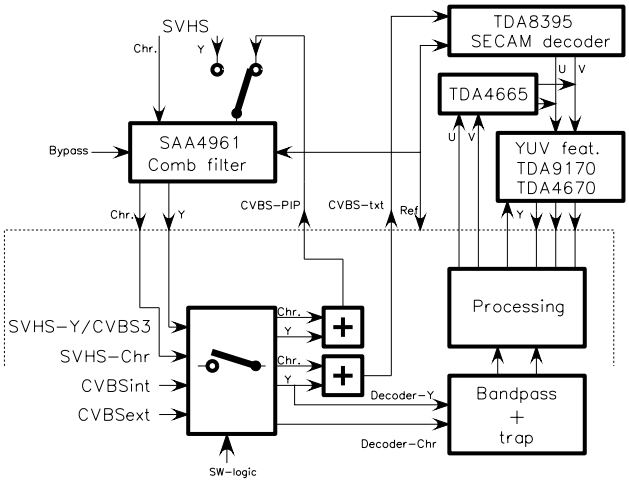


Figure 4 Source selector, comb filter and YUV feature connections.

2.3. Horizontal synchronization and protection.

The synchronizing separator adapts its slicing level to the middle of the top-sync pulse and the black level of the $CVBS_{TXT}$ signal. The separated synchronizing pulses are fed to the first phase detector (ϕ1-loop) and to the coincidence detector. The ϕ1-loop gain is determined by the components at pin 44 (C + RC). The coincidence detector detects whether the horizontal line oscillator is synchronised to the incoming video. The line oscillator is a VCO-type, running at twice the line frequency. It is calibrated using the Xtal oscillator frequency of the colour decoder and has a maximum deviation of 2% of the nominal frequency, so no alignment is needed. Because of the calibration procedure, it has to be indicated which crystals are connected to the oscillator pins by using bits **XA** and **XB** (see chapter 2.10.1 on page 19). The calibration takes place after start-up and also after synchronization loss (ϕ1 coincidence detector bit **SL**).

The time constant of the ϕ1-loop can be switched via the I²C bus (**FOA,FOB**), fast or slow. In normal mode the time constant is automatically chosen depending on the noise content of the video signal.

The second phase detector ϕ2 locks the phase of the horizontal driver pulses at the horizontal output pin (pin 40) to the horizontal flyback pulse present at pin 41. This compensates for the storage time of the horizontal deflection transistor. The ϕ2-loop filter (C) is externally connected to pin 43. The horizontal phase can be given a static offset via I²C-bus (**HSH**). A dynamic phase correction is possible by current feedback into the ϕ2-loop filter capacitor (e.g for EHT compensation).

To protect the horizontal deflection transistor, the horizontal drive is switched off immediately when a power failure (”Power-On Reset” bit **POR**) is detected. The power failure may have corrupted the contents of the internal data registers, so the start up procedure for the TDA8376(A) should done again (see chapter 2.10.1 on page 19). The horizontal drive output is gated with the flyback pulse to prevent the horizontal output transistor from switching on during flyback time.

During switch-on and switch-off the horizontal output frequency is doubled, this results in a smooth switch on/off behaviour of the horizontal output stage.

For overvoltage protection the EHT compensation input pin 49 is used. The EHT compensation input range is 1.2 .. 2.8V, above 3.9V the overvoltage protection bit **XPR** is set (detection, **PRD**=0). When the over-voltage protection is enabled (bit **PRD**=1), the horizontal driver pulses are stopped (protection). Note that **XPR** has no latch function, so when the over-voltage condition is gone, the horizontal drive starts again via a slow start procedure.

An additional ”flash” protection can be implemented at ϕ2-loop filter pin 42. A level above 6 Volt will immediately switch off the horizontal driver pulses. The slow start procedure is activated after the pin 42 voltage sinks below the flash protection level of 6V.
Note that if **POR** was triggered too, the TDA8376(A) waits until the status bytes are read.

The TDA8376(A) has a separate supply input (pin 37) for the horizontal oscillator circuits, used for seperate decoupling of these circuits. The main supply (pin 8) must be present to start the horizontal oscillator, because it is only possible to start the horizontal oscillator via the I²C-bus. The internal I²C-bus is supplied via pin 8.

2.4. Vertical synchronization.

The vertical sawtooth generator drives the vertical output and East-West correction drive circuits. It uses an external capacitor at pin 50 and a current reference resistor at pin 51.
The TDA8376(A) vertical drive has differential current outputs for DC-coupled vertical output stages, like the TDA8350/51A/56. At the TDA8350/51A/56 input pins 1 and 2 this current is converted into a drive voltage via a resistor of 3kΩ.
To avoid damage to the picture tube when the vertical deflection fails, the guard output pulses of the TDA8350/51A/56 are connected to the sandcastle input (pin 39) of the TDA8376(A). When the vertical guard pulses are missing, bit **NDF** is set (detection). Dependant on bit **EVG** the RGB_{OUT} pins are blanked (protection).
Vertical de-interlace for teletext purposes can be set via bit **DL**.

2.5. Geometry processing.

The geometry processor of the TDA8376(A) offers the following controls:

- Horizontal shift (HS)
- E-W amplitude (EW)
- E-W parabola width (PW)
- E-W corner parabola (CP)
- E-W trapezium (TC)
- Vertical slope (VS)
- Vertical amplitude (VA)
- Vertical S-correction (SC)
- Vertical shift (VSH)

All of these parameters can be controlled via the I²C bus, which means that automatic geometry alignment can be used with this concept.
A single ended output (pin 46) is provided for the E-W drive. This output is a linear current output (open collector type). Both the E-W and vertical drive outputs can be modulated for EHT compensation (pin 49). The EHT tracking mode bit **HCO** can select to modulate only vertical or vertical and E-W. The 'Only vertical' mode is useful when fast feedback for E-W and slow feedback for vertical is desired. Then the fast E-W feedback can be made outside the chip. It also can be used in concepts with raster correction free tubes.

The second function of the EHT compensation pin 49 is over-voltage protection and/or detection (see chapter 2.3 on page 12).

The geometry processor of the TDA8376 also offers the possibility for vertical compression (for display of 16:9 pictures on a 4:3 screen) or vertical expansion (for display of 4:3 pictures on a 16:9 tube, with full picture width). In case of subtitles in the expand mode, it is also possible to lift the picture up (expand and lift mode). These modes can be chosen via I²C bus bits **EXP** and **CL**.
The geometry processor of the TDA8376A has the possibility for linear zoom. Therefore an extra I²C bus register is used for vertical zoom (**VX** sub address 16) and the horizontal width (**EW**) control range is extended.

2.6. Colour decoder.

The colour decoder contains an alignment-free Xtal oscillator, a dual killer circuit and colour difference demodulators. The decoder automatically adapts for PAL and NTSC signals. Together with the TDA8395 SECAM add-on a multi standard PAL/SECAM/NTSC decoder can be built, with automatic standard recognition. The recognized colour standard can be read via status bits **CD0..CD2**. It is also possible to force the TDA8376(A) to a colour standard via bits **CM0..CM2**. Which standard can be decoded depends on the external Xtals used. Two Xtal pins (33 and 34) are present, so normally no external switching is required. The IC must be told which Xtals are connected (bits **XA** and **XB)**. This is important, because the Xtal frequency of the colour decoder is also used to calibrate the horizontal oscillator (see chapter 2.10.1 on page 19).

The burst phase detector locks the Xtal oscillator with the chroma burst signal. The phase detector operates during the burst key period only, to prevent disturbance of the PLL by the chroma signal. Two gain modes provide:
- Good catching range when the PLL is not locked.
- Low ripple voltage and good noise immunity once the PLL has locked.

The killer circuit switches-off the R-Y and B-Y demodulators at very low input signal conditions (chroma burst amplitude). A hysteresis prevents on/off switching at low, noisy signals.

Colour standards	Pin 33	Pin 34	XA	XB	Remark
NTSC-M + PAL-M or N	3.58	3.58	0	0	Two 3.58 MHz standards
NTSC-M or PAL-M or N	3.58	none	0	1	One 3.58 MHz standard
NTSC-4.4 + PAL-4.4 + SECAM	none	4.43	1	0	4.43 for PAL/SECAM/NTSC
NTSC-M + NTSC4.4 + PAL-4.4 + SECAM	3.58	4.43	1	1	One 3.58 + one 4.43 standard
NTSC-M + PAL-M + PAL-N [1)]	3.58	M+N	0	0	External switch between M/N

Table 2. Colour Xtal applications for TDA8376(A).

Note [1)]: The switching between PAL-M and PAL-N should be done externally via two transistors. To avoid calibration problems, the configuration should temporarily be set to only one 3.58 Xtal on pin 33 (bit **XA**,**XB**=0,1), while the Xtals on pin 34 are being switched.

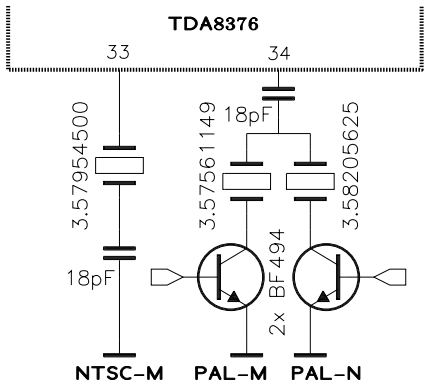


Figure 5 Combining NTSC-M, PAL-M and PAL-N

2.7. Integrated video filters.

The TDA8376(A) has alignment-free internal luminance delay, chroma bandpass and chroma trap. They are implemented as gyrator circuits, tuned by tracking to the selected frequency of the chroma Xtal oscillator.
The chroma trap in the Y signal path is by-passed when Y/C input is selected (S-VHS).
An adjustable delay for the luminance signal is available, to correct the delay, when e.g. the SAW filter is not according to the standard. This delay can be set via I²C bus by using bits **YD0-YD3**.
In SECAM mode the centre frequency of the chroma trap is set to a value of approximately 4.2 MHz to obtain a better suppression of the modulated colour subcarriers.
On the TDA8376(A) Y_{OUT} and Y_{IN} are available at pin 28 and 27. Together with the R-Y and B-Y outputs and inputs, various YUV features can be inserted, like PIP, PSI (TDA4670) or the TDA9170 picture booster.

2.8. Black-stretcher circuit.

The TDA8376(A) is provided with a black stretcher cicuit in the luminance channel. It can stretch the luminance signals below 50 IRE. It streches a peak black level found in the luminance signal to the black level found on the back porch of the video signal. The circuit can be switched off by connecting pin 2 to the positive supply line.

2.9. RGB output and black-current stabilisation.

The colour difference signals (R-Y, B-Y) are matrixed with the luminance signal (Y) to obtain the RGB_{OUT} output signals (pins 21,20,19). In the TDA8376(A) the matrix type automatically adapts to the decoded standard (NTSC/PAL) but it can be forced to the PAL matrix via I²C bus bit **MAT**.

There are two RGB inputs at pins 23,24,25 and pins 15,16,17. One of these can be chosen to be displayed. Linear amplifiers are used to interface one of these external RGB_{INPUT} signals. These signals overrule the internal RGB signals when the data insertion pin 26 (FBl_1), or 14 (FBl_2) is switched to a level between 1.0V and 3.0V. The insertion pins have a second detection level at 4V. Above this level the RGB_{OUT} pins are switched to black level. In this way on-screen display (O.S.D.) signals can be supplied directly to the inputs of the video output stages without any interaction with the RGB of the colour decoder part.
RGB insertion directly at the RGB_{OUT} pins of the TDA8376(A) is also possible, but the automatic black current stabilisation may cause a difference in white balance between OSD/TXT and the main picture.
The RGB(2) inputs (pins 15,16,17) have priority against the RGB(1) inputs (pins 23,24,25). So in most applications RGB(1) inputs are used for SCART RGB input and RGB(2) inputs are used for OSD/TEXT inputs.
Both RGB inputs can be blocked by means of I²C bus bits (**IE1**, **IE2**). The activity of the fast blanking signals can be read via I²C status bits **IN1** and **IN2**.

The contrast and brightness control and the peak white limiter operate on both internal and external RGB signals. R,G and B each have their own, independent, ”gain” control, to set the correct white point and to compensate for the difference in phosphor efficiencies between picture tubes. The nominal amplitude is about 2V black to white, at nominal input signals and control settings.

The TDA8376(A) has a black current stabilisation loop, that automatically adjusts the black level to the cut-off voltage of the picture tubes three gun cathodes. Since no current is flowing when the voltage on the cathode is equal to the cut-off voltage of the tube, the loop stabilizes at a very small gun current. This ”black current” of the three guns is measured internally and compared with a reference current, to adjust the black level of RGB_{OUT}. The black level loop is active during 4 lines at the end of the vertical blanking. In the first line the leakage current is measured (max. acceptable $\pm$ 100 μA). In the next three lines the black levels of the three guns are adjusted. The nominal value of the ”black current” is 10 μA. The ratio of the ”black currents” for the 3 guns tracks automatically with the white point adjustment, so the back-ground colour is the same as the adjusted white point.

At switch-on of the TV receiver the black current stabilisation circuit is not yet active and RGB_{OUTs} are blanked. Before the first measurement pulses appear, 0.5 s delay ensures that the vertical deflection is active, so the pulses will not be visible on the screen. During the measuring lines RGB_{OUT} will supply 4 V pulses to the video output stages. The TDA8376(A) waits until the black current feedback input (pin 18) exceeds 200 μA, which indicates that the picture tube is warm. Then the black current stabilisation circuit is activated. After a waiting time of about 1.0 s. the blanking of RGB_{OUT} is released.

2.10. I²C bus description.

Input functions[1] (write)		Sub addr. (hex)	Data bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Source select		00	INA	INB	INC	IND	FOA	FOB	XA	XB[5]
Decoder mode		01	FORF	FORS	DL	STB	POC	CM2	CM1	CM0
Hue	HUE	02	0	0	A5	A4	A3	A2	A1	A0
Horizontal shift	HSH	03	0	0	A5	A4	A3	A2	A1	A0
E-W width	EW	04	0	0	A5	A4	A3	A2	A1	A0
E-W parabola correction	PW	05	0	0	A5	A4	A3	A2	A1	A0
E-W corner correction	CP	06	0	0	A5	A4	A3	A2	A1	A0
E-W trapezium correction	TC	07	0	0	A5	A4	A3	A2	A1	A0
Vertical slope	VS	08	NCIN	0	A5	A4	A3	A2	A1	A0
Vertical amplitude	VA	09	VID	LBM	A5	A4	A3	A2	A1	A0
S-correction	SC	0A	HCO	EVG	A5	A4	A3	A2	A1	A0
Vertical shift	VSH	0B	SBL	PRD	A5	A4	A3	A2	A1	A0
White point Red	WPR	0C	EXP[2]	CL[2]	A5	A4	A3	A2	A1	A0
White point Green	WPG	0D	0	CVS	A5	A4	A3	A2	A1	A0
White point Blue	WPB	0E	MAT	0	A5	A4	A3	A2	A1	A0
Peaking	PEAK	0F	YD3	YD2	YD1	YD0	A3	A2	A1	A0
Brightness	BRI	10	RBL	COR	A5	A4	A3	A2	A1	A0
Saturation	SAT	11	IE1	IE2	A5	A4	A3	A2	A1	A0
Contrast	CON	12	0	0	A5	A4	A3	A2	A1	A0
Spare		13	0	0	0	0	0	0	0	0
Spare		14	0	0	0	0	0	0	0	0
Spare		15	0	0	0	0	0	0	0	0
Vertical zoom[3]	VX	16	0	0	A5	A4	A3	A2	A1	A0
Output functions (read)		Sub addr.	Data bits							
Status byte 0		00	POR	FSI	STS	SL	XPR	CD2	CD1	CD0
Status byte 1		01	NDF	IN1	IN2	IFI	AFA	X	SXA	SXB

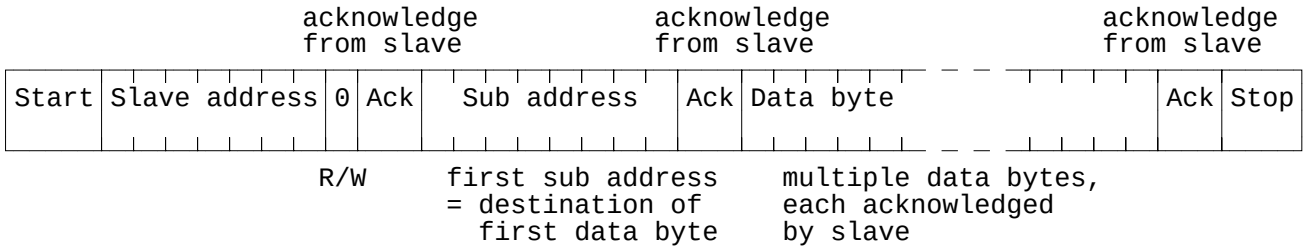
Table 3. I²C-bus functions of the TDA8376(A).

Note: [1] All not-used bits should be set to zero, for compatibility with future devices.
[2] Only valid for TDA8376, must be set to 0 for TDA8376A.
[3] Only valid for the TDA8376A, must be zero for the TDA8376, or do not write the last four registers.

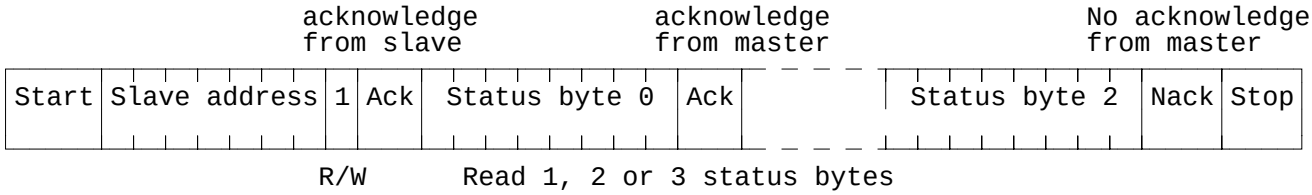
The TDA8376(A) needs only two I²C-bus pins (4=SDA and 3=SCL) to read and write all its functions:

- Write slave address: $8A_{HEX}$: A6 A5 A4 A3 A2 A1 A0 R/W : 1 0 0 0 1 0 1 0
- Read slave address: $8B_{HEX}$: A6 A5 A4 A3 A2 A1 A0 R/W : 1 0 0 0 1 0 1 1

For I²C-bus write-transmissions the TDA8376(A) has automatic sub-address increment, so multiple data bytes can be sent in one transmission.



Reading the three status bytes is done without sub addressing. After receiving the I²C-bus read address, the TDA8376(A) always starts with status byte 0.



2.10.1. I²C-bus start-up procedure.

The TDA8376(A) has many alignment-free internal circuits that are calibrated with the frequency of the colour Xtal oscillator. At start-up an I²C-bus write-message has to tell which type of Xtals are connected to pins 33 and 34 (bits **XA** and **XB**). Validity of this selection is essential, therefore the following start-up procedure should be implemented in the software:

•1 Keep reading the I²C-bus status bytes, until **POR**=0.
•2 Write all sub address bytes, with correct values for **XA** and **XB**.

The horizontal drive output becomes active after sub address bytes 00_{HEX} to 13_{HEX} are loaded and the oscillator is calibrated.

Each time before the sub address bytes are refreshed, the status bytes must be read. If **POR**=1 then the start-up procedure must be carried out to restart the IC. Not following this procedure may result in undesired conditions after power-up or a power dip (e.g. incorrect horizontal line frequency).

The **AFA** status bit indicates which device is operating in the receiver, either TDA8376 (**AFA**=0) or TDA8376A (**AFA**=1).

2.10.2. Synchronisation part.

Input: **XA / XB** : Indication which Xtals are connected to the oscillator pins: The Xtal oscillator frequency is used to calibrate the horizontal frequency. Therefore the software must indicate which Xtals are connected, before calibration takes place.

XA	XB	Pin 33	Pin 34
0	0	3.58 MHz	3.58 MHz
0	1	3.58 MHz	None
1	0	None	4.43 MHz
1	1	3.58 MHz	4.43 MHz

POC : Synchronisation mode: When this bit is switched to high, the ϕ1-loop is switched off completely. In this mode very stable OSD or TEXT can be displayed. It is also possible to measure the free running frequency in this way.
0 = Synchronisation active
1 = Synchronisation not active

FOA / FOB : ϕ1 time constant: These two bits determine the speed of the ϕ1-loop. It can be in the automatic mode or forced to slow and fast. In auto mode a noise detector circuit can switch to the slow time constant, when the signal has too much noise.

FOA	FOB	ϕ1-loop mode
0	0	Auto
0	1	Slow
1	X	Fast

VID : Video ident mode: With this bit it is possible to activate a coupling between video ident (**IFI**) and ϕ1-loop. If this coupling is active and no video is present, the ϕ1-loop is switched to very slow. This assures a stable OSD display.
When **IFI** is not coupled to the displayed video source, **VID** should be set high.
0 = Video ident switches ϕ1-loop on/off
1 = No influence of the video ident on the ϕ1-loop

LBM : Long blanking mode: This bit sets the 60 Hz vertical blanking interval to the 50 Hz standard. In certain 50/60 Hz applications this can simplify the vertical output stages, regarding the maximum vertical retrace time. With a fixed blanking time, visible vertical retrace lines can be avoided.
0 = Blanking adapted to standard (50 or 60 Hz)
1 = Fixed blanking according to 50 Hz standard

DL : Interlace: This can switch off the interlace, e.g. for TEXT applications.
0 = Interlace
1 = De-interlace

HCO : EHT tracking mode: Selects to modulate only vertical or vertical and E-W with the information on pin 49. EHT tracking compensates picture size variations due to beam current variation. **HCO** = 0 is useful when E-W and vertical require different speeds of the feedback. Slow feedback for vertical can then be done via the TDA8376(A), while fast E-W feedback is made outside the IC.
0 = EHT tracking only on vertical
1 = EHT tracking on both vertical and East-West

FORF / FORS : Forced field frequency: This forces the vertical divider in a 60 Hz mode or automatic. In auto mode it can be given a preference for 50 or 60 Hz or to keep the last detected field frequency.

FORF	FORS	Vertical frequency
0	0	Auto, 60 Hz if not locked
0	1	60 Hz forced[1)]
1	0	50 Hz forced[1)]
1	1	Auto, 50 Hz if not locked

Note: [1)] When already locked at 50 Hz, 60 Hz will be forced after the first sync loss.

NCIN : Vertical divider mode: Normally the TDA8376(A) switches automatically back to large window after three missing vertical sync. pulses when it was in standard mode, or after maximally six missing sync. pulses when it was in standard TV-norm mode. At channel change a quick forcing to search mode speeds up vertical catching. After video ident. the vertical divider can be switched back to normal operation.
0 = Normal operation of the vertical divider
1 = Vertical divide switched to large, search mode

EVG : Enable vertical guard, see chapter 2.10.7 on page 26.

SBL : Service blanking: This bit can blank the bottom half of the picture, starting exactly in the middle of the vertical scan. This can be used to align the vertical parameters.
0 = No service blanking
1 = Service blanking active

Output: **SL** : Horizontal lock indication:
0 = Not locked
1 = ϕ1-loop locked to the incoming video signal

IFI : Output of video ident circuit.
0 = No video signal identified
1 = Video signal identified

FSI : Field frequency indication: Selected vertical frequency.
0 = 50 Hz
1 = 60 Hz

NDF : Vertical guard output, see chapter 2.10.7 on page 26

SXA / SXB : These bits give the status of the XA and XB X-tal indication bits, so the software can check if I²C bus transmission of these bits was succesful. Since the horizontal oscillator uses these bits for calibration, it is important they have the correct value.

XA	XB	Pin 33	Pin 34
0	0	3.58 MHz	3.58 MHz
0	1	3.58 MHz	None
1	0	None	4.43 MHz
1	1	3.58 MHz	4.43 MHz

2.10.3. RGB output stages and vertical functions.

Input: **RBL** : RGB blanking:
0 = Normal picture visible
1 = RGB_{OUT} (pins 21,20,19) blanked

IE1 : Enable fast blanking: When this bit is low, the fast blanking function of pin 26 is disabled, so no external RGB_{IN} insertion at pins 23,24,25 is possible.
0 = Fast blanking disabled
1 = Normal fast blanking function

IE2 : Enable fast blanking: When this bit is low, the fast blanking function of pin 14 is disabled, so no external RGB_{IN} insertion at pins 15,16,17 is possible.
0 = Fast blanking disabled
1 = Normal fast blanking function

EXP/CL : Vertical mode (TDA8376 only): These bits offer the possibility to adapt the vertical deflection, to display a 16x9 signal on a 4x3 tube and visa versa.

EXP	CL	mode
0	0	normal
0	1	compress
1	0	expand
1	1	expand + lift

Output: **IN1** : Reflects the level on the fast blanking input pin 26:
0 = Pin 26 above insertion level (>0.9V, RGB_{IN} inserted when **IE1**=1)
1 = Pin 26 low (< 0.3V), no insertion

IN1 : Reflects the level on the fast blanking input pin 14:
0 = Pin 14 above insertion level (>0.9V, RGB_{IN} inserted when **IE2**=1)
1 = Pin 14 low (< 0.3V), no insertion

2.10.4. Source switches and luminance processing.

Input: **INA / INB / INC / IND** : Input source select switch: This determines which video signal is displayed and available at $CVBS_{OUT}$ pin 38 and which video signal is available at pin 11 (PIP output). The output at pin 38 can be used to for teletext and the TDA8395 SECAM add-on. The output at pin 11 can be used for PIP or a COMB filter.

INA	INB	Selected video source		CVBS switch output (pin 38) and display
0	0	$CVBS1_{INT}$	pin 9	$CVBS1_{INT}$
0	1	$CVBS3_{EXT}$	pin 13	$CVBS3_{EXT}$
1	0	Y,C_{S-VHS}	pins 7, 6	Y + C added
1	1	Y,C_{S-VHS} ($CVBS_{EXT}$ [1])	pins 7, 6	Y + C added (or $CVBS_{EXT}$)

INC	IND	Selected video source		CVBS PIP output (pin 11)
0	0	$CVBS1_{INT}$	pin 9	$CVBS1_{INT}$
0	1	$CVBS3_{EXT}$	pin 13	$CVBS3_{EXT}$
1	0	Y,C_{S-VHS}	pins 7, 6	Y + C added
1	1	Y,C_{S-VHS} ($CVBS_{EXT}$ [1])	pins 7, 6	Y + C added (or $CVBS_{EXT}$)

Note: [1] $CVBS_{EXT}$ will be displayed if no SVHS signal is available (detected by sync. presence at pin 7)

CVS : Condition Y/C input: by setting this bit high, the SVHS luminance input (pin 7) can be used as a CVBS input, offering more switching possibilities
0 = input set to S-VHS luminance mode.
1 = input set to CVBS mode

COR : Noise coring: This bit reduces the peaking function on small transients. Coring is not reducing the noise, but in scenes with little contrast it prevents the peaking from making the noise very visible.
0 = Noise coring off
1 = Noise coring on

YD0-YD3 : Luminance to chrominance delay setting: these bits offer the possibility to correct the Y - chroma delay for different colour standards.
YD3 adds 160 ns delay.
YD2 adds 80 ns delay.
YD1 adds 40 ns delay.
YD0 adds 40 ns delay.

Output: **STS** : S-VHS status: this bit is set high, when a sync. signal is present at the S-VHS luminance input (pin 7).
0 = No sync. present
1 = sync. present

2.10.5. Colour decoder.

Input: **MAT** : PAL/NTSC matrix: Forces PAL matrix, even when NTSC is detected.
0 = Matrix adapted to standard (Japanese NTSC matrix or PAL matrix)
1 = Forced to PAL matrix

CM2..CM0 : Colour decoder mode: With these bits the automatic mode can be selected or the decoder can be forced to one of the standards. Xtal selection bits **XA** and **XB** should not be contradictory to a forced Xtal selection in the colour decoder mode (e.g. force pin 35 while there is only a Xtal on pin 34).

CM2	CM1	CM0	Colour decoder mode
0	0	0	Automatic, own intelligence, 2 Xtals
0	0	1	Forced NTSC 3.58
0	1	0	Forced PAL 4.43
0	1	1	Forced SECAM (4.43)
1	0	0	Forced NTSC 4.43
1	0	1	Forced PAL 3.58, pin 33
1	1	0	Forced PAL 3.58, pin 34
1	1	1	not used

Output: **CD2..** Colour detection: Reflects the colour standard that is identified by the TDA8376(A).
CD0 :

CD2	CD1	CD0	Colour standard
0	0	0	No colour standard identified
0	0	1	NTSC, 3.58 MHz
0	1	0	PAL, 4.43 MHz
0	1	1	SECAM via TDA8395
1	0	0	NTSC 4.43 MHz
1	0	1	PAL 3.58 MHz, pin 33
1	1	0	PAL 3.58 MHz, pin 34
1	1	1	Not used

2.10.6. Analogue controls.

The parameters in the table below are just rough indications and may change without notice. Please consult the TDA8376(A) device specification (ref.[1]) for the most up-to-date values.

Function		Sub address$_{HEX}$	Steps	Range			
Hue	HUE	02	63	-40 ..	+40	°	
Horizontal shift	HSH	03	63	-2 ..	+2	µs	
E-W width	EW	04	63	100 ..	80	%	
E-W parabola width	PW	05	63	0 ..	24	%	
E_W corner parabola	CP	06	63	-44 ..	0	%	
E-W trapezium	TC	07	63	-4 ..	+4	%	
Vertical slope	VS	08	63	-14 ..	+14	%	
Vertical amplitude	VA	09	63	80 ..	120	%	1)
S-correction	SC	0A	63	0 ..	25	%	
Vertical shift	VSH	0B	63	-4 ..	+4	%	
Vertical zoom (only TDA8376A)	Vx	16	63	75 ..	138	%	2)
White point R,G and B	WPR,G,B	0C,0D,0E	63	-50 ..	+50	%	3)
Peaking	PEAK	0F	15	0 ..	40	%	
Luminance-Chrominance delay	YD	0F	15	-160 ..	+160	ns	
Brightness	BRI	10	63	-0.7 ..	+0.7V		4)
Saturation	SAT	11	63	0 ..	250 %		
Contrast	CON	12	63	10 ..	100 %		

Table 4. Analogue control functions of the TDA8376(A).

Note: 1) Valid when SC = 00_{HEX}, for SC = $3F_{HEX}$ the range is 86 .. 112%.
2) Nominal setting = 19_{HEX}.
3) Nominal setting = 20_{HEX}.
4) Relative variation with respect to black at RGB_{OUT}.

2.10.7. Power and protection.

Input: **STB** : Standby: After power on, the bit is low and should only be set high **after the start-up procedure of chapter 2.10.1** (see page 19).
0 = TDA8376(A) in standby mode
1 = IC operational

PRD : Over-voltage protection input mode: When the bit is high, an over-voltage situation will stop the horizontal drive (and set bit **XPR**). If a complete switch off of the system is desired, the micro processor should activate the stand-by bit **STB**, otherwise the horizontal drive can start again.
0 = Only over-voltage detection (output bit **XPR**)
1 = Over-voltage detection (**XPR**) and inhibit horizontal drive (protection)

EVG : Enable vertical guard: With this bit set high, a vertical guard failure will immediately blank RGB_{OUT} to avoid damage to the picture tube.
0 = Only vertical guard detection (output bit **NDF**)
1 = Detection (**NDF**) and protection by blanking RGB_{OUT}

Output: **POR** : Power on reset: Indicates detection of a power failure. It remains high until the status bytes have been read successfully. When a failure is detected, the internal data is not reliable any more and should be refreshed. During normal operation the POR status should be read continuously, before sending any input data. During start-up, the IC status should be read until the POR bit is low, immediately followed by sending all register data (see start-up procedure of chapter 2.10.1, page 19).
0 = Device operational
1 = Power failure detected

XPR : Overvoltage protection:
0 = No over-voltage detected
1 = Over-voltage detected on EHT input pin 49

NDF : Vertical guard output:
0 = Vertical deflection OK
1 = Failure detected in the vertical output stage via pin 39

3. Demonstration board circuit description.

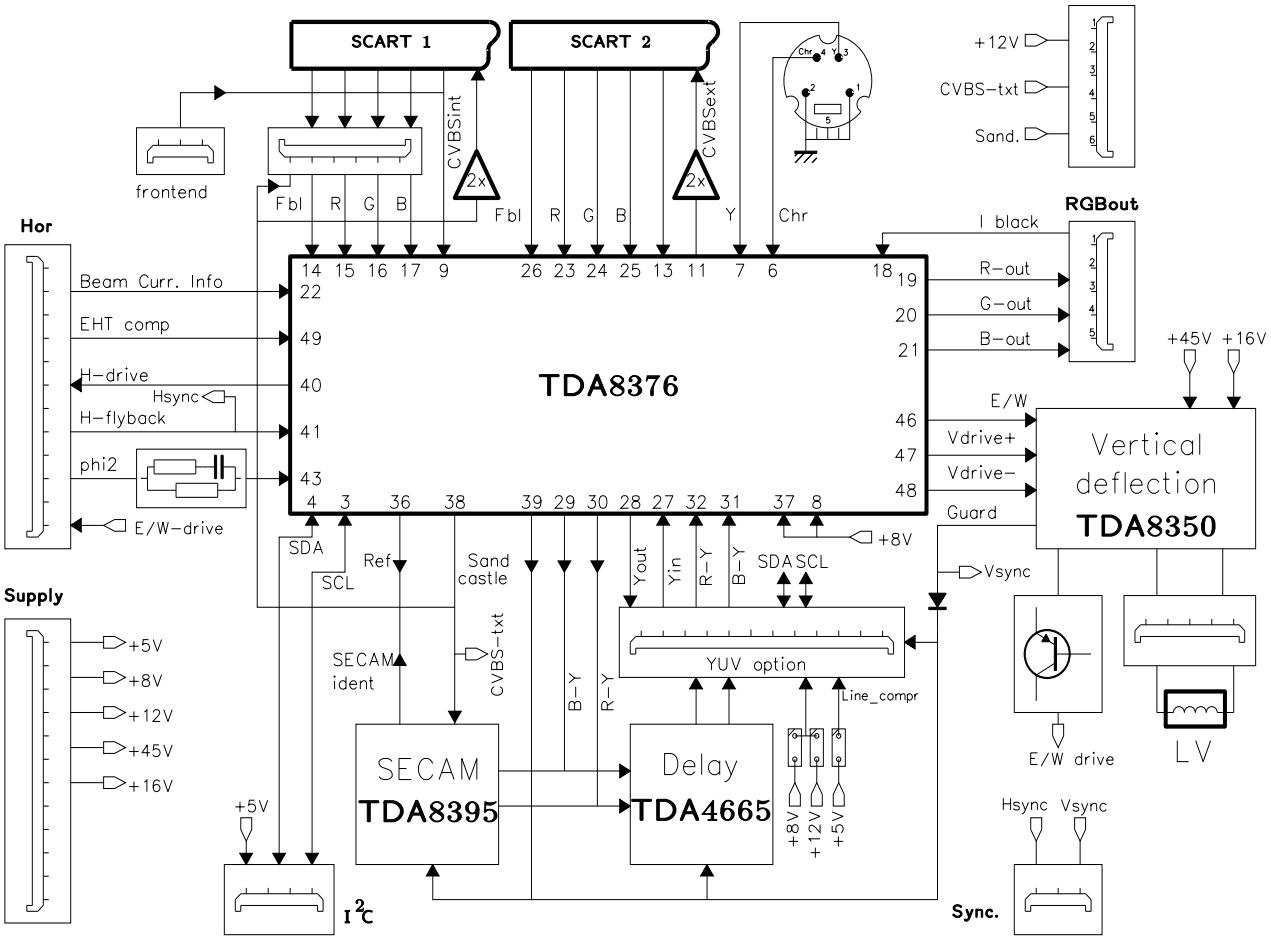


Figure 6 Block diagram of TDA8376(A) demo board PR32031.

The TDA8376(A) demonstration board PR32031 (see figures on this page, pages 39, 40 and 41) is in principal not a complete receiver. It has no tuner, horizontal deflection, power supply, sound and micro controller part. The board shows a practical layout, that can be used as an example for new receiver designs. However, it is not optimised nor tested for EMC performance.

When connected to the CRT and power supply boards, listed on page 8, PR32031 becomes a complete monitor with two scart inputs.

The demonstration board is suited for PAL 4.43, NTSC 4.43/3.579 and SECAM input signals.
The receiver has two full scarts ($CVBS_{IN,OUT}$, RGB_{IN}) and an S-VHS input.
The CVBS output at scart-1 is the same as the decoded CVBS signal. The CVBS output at scart-2 can be chosen freely amongst the available input sources (CVBS-PIP output).

The vertical deflection uses the TDA8350 DC-coupled vertical output stage (see chapter 3.4, page 30), that has an East-West output amplifier to drive an E-W modulator for the horizontal deflection. For applications without E-W, the pin-compatible (13 pins) TDA8351A can be used. The TDA8356 is also recommended for use with TDA8376(A), but it does not fit on the demonstration board because the pinning (9 pins) is different. The vertical deflection coil can be connected to plug "VERT".
For demonstration without vertical deflection coils, the vertical guard should be disabled via bit **EVG**.

3.1. TDA8395 SECAM decoder.

The TDA8395 is an alignment-free SECAM colour decoder, including a Cloche filter, demodulator and line identification circuit. Few external components are needed because of internal calibration.
For detailed information about TDA8395 application, see ref.[8].

The Cloche filter is a gyrator-capacitor type. Its frequency is calibrated in the vertical retrace period. The calibration reference (pin 1) is obtained from the TDA8376(A) colour Xtal oscillator (pin 36). Pin 7 is a decoupling for the Cloche reference. The voltage change at this pin due to leakage currents should be lower than 10 mV, during field scan, resulting in a capacitor of minimal 100 nF. The capacitor decoupling loop to ground pin 6 should be kept short and clean.
Pin 8 is the reference capacitor for the PLL. The voltage variation during field scan at this pin should be lower than 2 mV, resulting in a capacitor of 220 nF, assuming 20 nA leakage current. Again the ground connection must be short.

The sandcastle input (pin 15) is connected to TDA8376(A) pin 39 and is used for generation of the blanking periods and provides clock information for the identification circuit.
The CVBS source select output (TDA8376(A) pin 38) supplies SECAM chroma to pin 16 of the TDA8395. This is demodulated by a PLL demodulator, that uses the reference frequency at pin 1 and a bandgap reference to obtain the desired demodulation characteristic.

If the digital line identification in the TDA8395 detects SECAM, pin 1 will sink a current of 150µA out of TDA8376(A) $SECAM_{ref}$ pin 36. When the TDA8376(A) has not detected PAL or NTSC, it will respond by increasing the voltage at pin 33 from 1.5 V to 5 V. The TDA8376(A) colour difference outputs pin 30 and 29 will be made high-ohmic and the TDA8395 outputs pin 9 and 10 are switched on. These outputs will be disconnected and high-ohmic when no SECAM is detected for two frame periods. The demodulator will be initialised before trying again to identify SECAM.

3.2. Base band delay line TDA4665.

The TDA4665 is an integrated double baseband delay line of 64 µS. It couples to the TDA8376(A) and TDA8395 without any switches or alignments. The TDA4665 consists of two main blocks:

- Two delay lines of 64 µsec in switched capacitor technique
- Internal clock generation of 3 MHz, line locked to the sandcastle pulse

The TDA4665 can operate in three modes:

- For PAL it operates as a geometric adder to satisfy the PAL demodulation requirements
- In NTSC mode it reduces cross-luminance interference (comb-filtering)
- For SECAM it repeats the colour difference signal on consecutive horizontal scan lines.

A sandcastle pulse is supplied to pin 5. The top pulse voltage, which should not exceed 5 V, can be directly coupled to the 5 V sandcastle output of the TDA8376(A).
The R-Y and B-Y colour difference signals (from TDA8376(A) pins 30 and 29) are AC-coupled and clamped by the input stages at pins 16 and 14. An internal 6 MHz Current Controlled Oscillator is line locked via a PLL, to the sandcastle pulse at pin 5. This clock drives the delay lines to obtain the required 64 µsec. Sample and hold low pass filters suppress the clock signal. The original and the delayed signals are added, buffered and fed to the output pins 11 and 12. These are AC-coupled to the R-Y and B-Y colour difference input pins 32 and 31 of the TDA8376(A).

The TDA4665 needs a 5 V supply voltage on pin 1 for the digital part and on pin 9 for the analog part. The digital 5 V decoupling should go to pin 3 (digital ground) and the analog supply to pin 10 (analog ground), both via the shortest possible path.

3.3. YUV feature interface.

Figure 7 shows how YUV-based features like TDA9170 (Picture Booster/histogram analysis) can be connected to the YUV connector (with $YUV_{IN,OUT}$, I²C, supply and sandcastle) of the demonstration board.

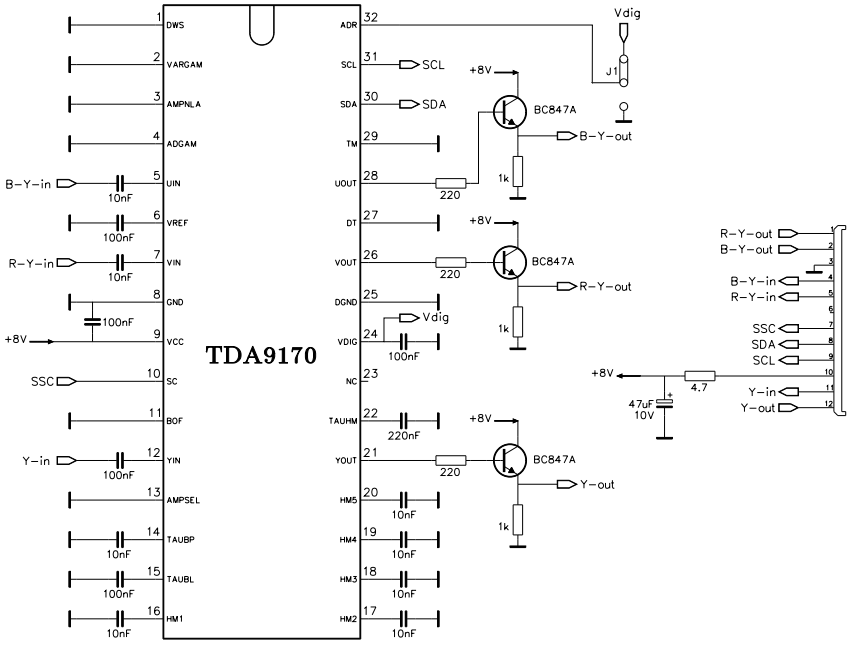


Figure 7 YUV feature connection for TDA9170.

Other examples of YUV based features are:

- TDA4566 Colour transient improvement + Y delay compensation
- TDA4670 Picture signal improvement
- PIP SAB9060, SAB9075/76 Picture In Picture insertion

With the $Y_{IN,OUT}$ of the TDA8376(A) it is also possible to make a second chroma trap at 4.3 MHz for improved SECAM applications.

3.4. TDA8350/51A/56 vertical deflection.

The TDA8350 is a combination of a vertical deflection circuit and an East-West amplifier. It can be used in 90° and 110° deflection systems with frame frequencies from 50 up to 120 Hz. With its bridge configuration the deflection output can be DC coupled with few external components. Only a single supply voltage for the scan and a second supply for the flyback are needed.
The East-West amplifier is used for driving the diode modulator in the horizontal deflection circuit. The TDA8351A and TDA8356 do not have an E-W amplifier. If required, they can be used with a discrete E-W amplifier directly driven by the TDA8376(A). The TDA8356 is intended for 90° systems.

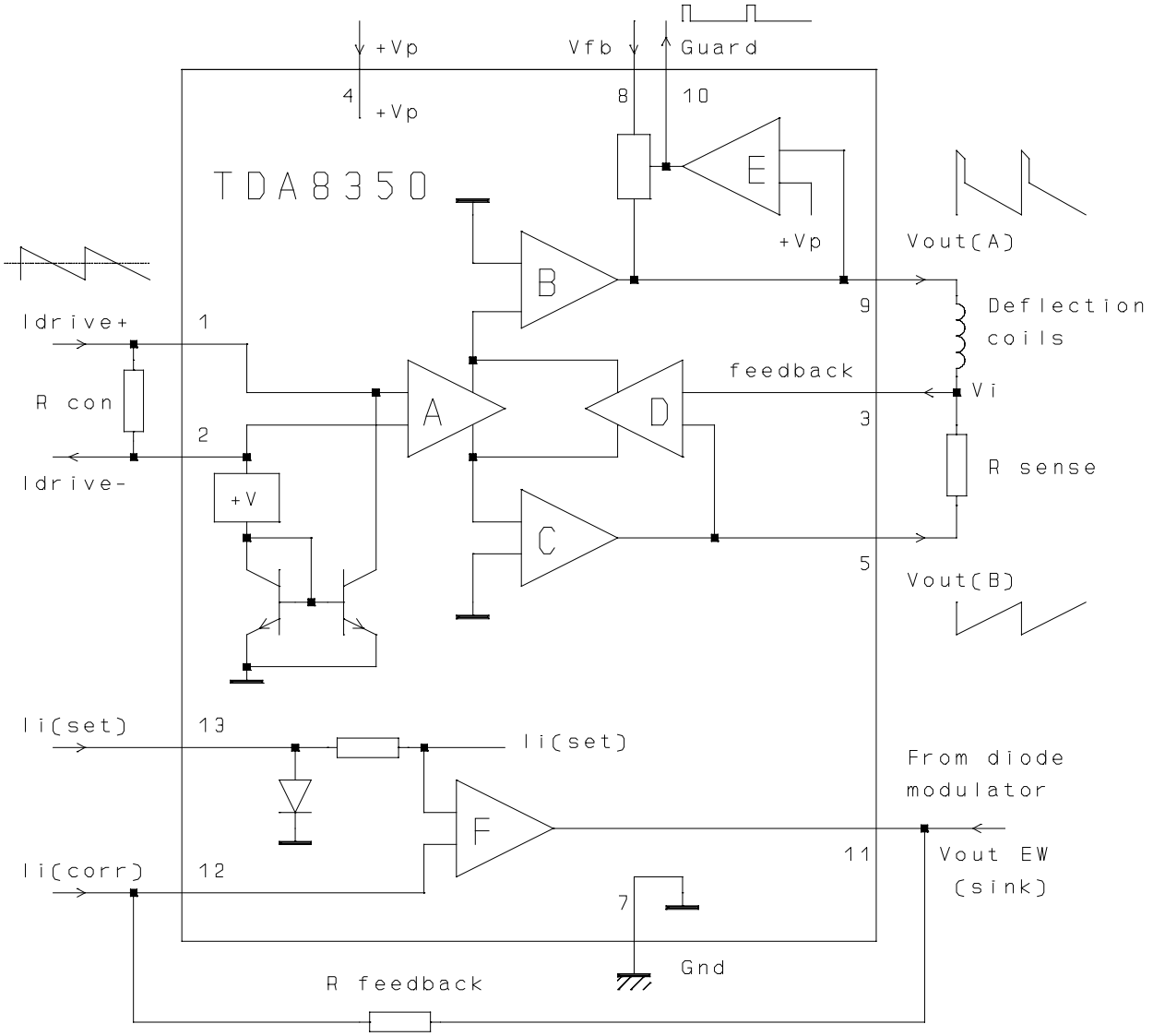


Figure 8 Block diagram of TDA8350.

The vertical drive currents at pins 48 and 47 are connected to input pins 1 and 2 of the TDA8350. The currents are converted into a voltage by a resistor between pins 1 and 2. Pin 2 is on a fixed DC level (internal bias voltage) and on pin 1 the drive voltage can be measured (typical 1.8 V_{PP}).

The drive voltage is amplified by ”A” and fed to two amplifiers ”B” and ”C” (see Figure 8), one is inverting and the other is a non inverting amplifier. The outputs (pins 5 and 9) are connected to the series connection of the vertical deflection coil and feedback resistor R_{SENSE}. The voltage across R_{SENSE} is fed via pin 3 to correction amplifier ”D”, to obtain a deflection current which is proportional to the drive voltage.

The supply voltage for the TDA8350 is 16V at pin 4. The flyback generator has a separate supply voltage of 45V on pin 8.

On pin 10 a vertical guard signal is available, which is obtained via amplifier ’E”. It is connected via a resistor to TDA8376(A) pin 22. When the vertical deflection is working correctly, the TDA8350/51A/56 produces a positive pulse during the vertical flyback interval. This is sensed by the TDA8376(A). In case of a disconnected coil, vertical power failure or malfunctioning TDA8350, the pulse will not be present. This condition can be read via bit **NDF**. To protect the picture tube against burn-in, the RGB_{OUT} pins will be blanked (unless the blanking protection was disabled by setting bit **EVG** = 0).

The guard pulse is also useful to synchronize OSD. For this reason a diode (with anode to pin 10) is added in series with the guard line (see Figure 13, page 41). A 10 kΩ resistor is connected (the load resistor may not exceed this value) from pin 10 to ground. Now a vertical sync pulse with 5 V amplitude is available over the 10 kΩ resistor.

Pin 46 of the TDA8376(A) drives East-West amplifier ”F”, whose gain can be set by resistor $R_{FEEDBACK}$. The amplifier output (pin 11) can be connected to a diode modulator circuit in the horizontal deflection part. In the demonstration board an extra buffer transistor and zener diode (33 V) are added to protect pin 11 against excessive high voltages and currents during a flash over of the picture tube.

3.5. Horizontal deflection.

In this chapter we will show how the horizontal deflection for TDA8376(A) can be made in principle. The circuit contains horizontal drive, line output transformer and diode modulator (see ref. [5]) circuit.

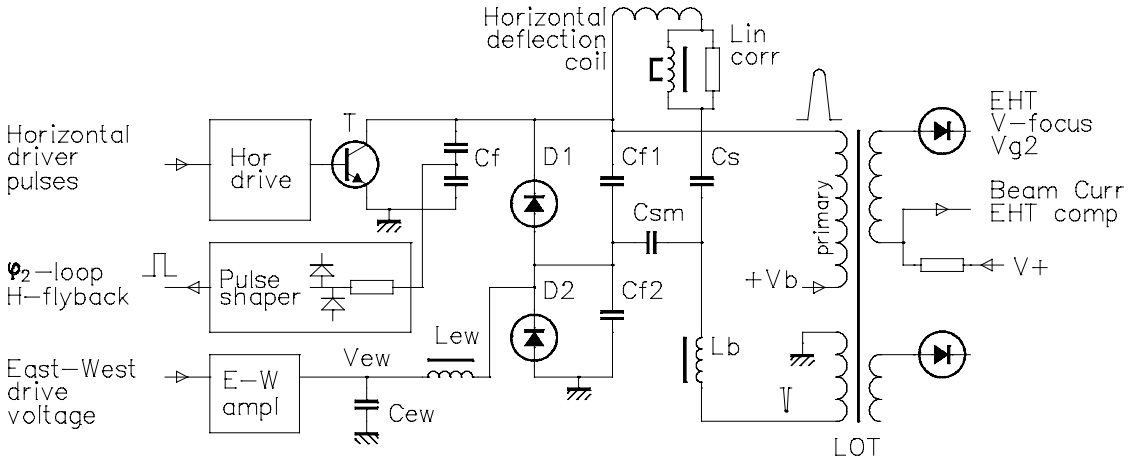


Figure 9 Functional diagram of horizontal deflection.

The horizontal drive pulses from the TDA8376(A) are amplified in the horizontal drive circuit, to get sufficient base-drive current for the high voltage switching transistor T. During the horizontal scan period (≈52 µs) T and/or D1,D2 will conduct, and a sawtooth current flows from +Vb through the primary winding of the LOT to ground. After this time T,D1,D2 are switched off and the energy stored in the LOT during the scan period will be transformed to the flyback capacitor Cf. This energy transfer will take place in a cosine shape because the primary of the LOT and Cf form a resonant circuit. The time the energy is transferred from LOT to Cf and back to the LOT, is called the flyback time and will take place in about 12µS. The flyback peak voltage is about 8 times the scan voltage.
From this pulse we derive a H-flyback pulse to close the ϕ2-loop. The pulse shaper can be e.g. a simple capacitive divider with two clipping diodes (from ground to H-flyback and from H-flyback to +8V). Note that the capacitor to ground is much larger than Cf, so that it does not affect the resonance. Another solution is to take the pulse from the collector, using a coupling capacitor with series resistor.

The diode modulator is modulating the horizontal deflection current without disturbing the amplitude of the flyback voltage on the primary of the LOT, thus the EHT voltage remains constant and independent of the horizontal deflection current (picture width). The diode modulator is formed by D1, D2, Cf1, Cf2, Lb and the Horizontal deflection coil. For a correct working of the diode modulator the resonance time of the following circuits must be equal:

- Cf with the primary inductance of the LOT
- Cf1 with the horizontal deflection coil
- Cf2 with Lb

The scan voltage for the LOT is Vb, for Lb it is Vew and for the deflection coil it is Vb-Vew. The scan voltage for the deflection coils can be changed by varying Vew with a constant Vb.

When the resonance frequencies of the separate tuned circuits are equal there will be no interaction between the tuned circuits during flyback and the total flyback voltage will always be about 8 times Vb. In series with the horizontal deflection coil there is a (damped) linearity corrector coil. During the scan there is some loss in the resistance of the deflection coil. In the first part of a line the linearity corrector stores some energy in a permanent magnet, until it is saturated. This improves the linearity of the horizontal scan speed.
The required S correction for the picture tube can be adjusted with the value of Cs. The modulated S correction (inner pincushion correction) can be adjusted with the value of Csm.

The modulating voltage Vew is obtained from the TDA8376(A) via the E-W amplifier in the TDA8350. Lew and Cew form a low-pass filter for the flyback pulses on the diode modulator, so that on the E-W amplifier only a frame frequent voltage is present.

The beam current limiting information (BeamCurr) and dynamic EHT compensation (EhtComp) are derived from the foot of the EHT winding of the LOT. This is connected via a resistor to V+. As the beam current increases, the voltage on line BeamCurr decreases. BeamCurr is damped by an integration filter before it is fed TDA8376(A) pin 22. The contrast and below 3V at pin 22 the brightness will be decreased to limit the average beam current.
AC information from the aquadag of the picture tube is added to the DC on line EhtComp. This combined information is fed via a filter to TDA8376(A) pin 50, for dynamic E-W correction. The time constant of the filter determines the dynamic behaviour of the EHT compensation.

The AC information can also be used to (pre)compensate for phase disturbances. Therefore this information needs to be inverted and fed to the $\phi 2$ loop capacitor of the TDA8376(A), pin 43.

3.6. Video amplifiers.

Three TDA6106 (pin aligned with TDA6101Q and TDA6111) integrated video amplifiers can drive the cathode of the picture tube directly. They are protected against CRT flash-over discharges and electrostatic discharge (ESD). For more information about integrated video amplifiers see ref. [4].

The three video amplifiers have a beam current output Iblack, used by the TDA8376(A) black current loop to control the black level on the cathodes.
The outputs can be connected together because the black current loop sequentially controls the black level for each cathode.

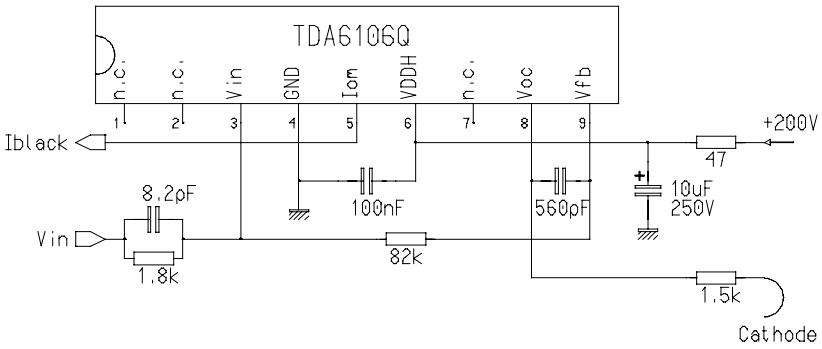


Figure 10 TDA6106 video amplifier.

The amplification of the TDA6106 is set by the resistors between pin 3 and 9 and between pin 3 (negative input) and the TDA8376(A) output, in this case: 68kΩ/1.5kΩ = 45.3 times.
The resistor from pin 3 to ground and the DC on TDA6106, pin 1 define an initial level on the cathodes for the black current stabilisation loop. In this example: 68kΩ/1.5kΩ•V_{pin1}=45.3•2.5=113 Volt.
There are no alignments any more on the CRT panel, because of the automatic black current stabilisation and because the white point adjustment can be done in the TDA8376(A) via I²C bus.

4. Application information.

4.1. Layout and EMC.

Special attention has been given to the layout of the demonstration board. The place and connection of some components is important for a good performance of the TDA8376(A) one chip. This chapter gives recommendations that can be helpful for the layout of TV receivers.

The demonstration board itself is not fully optimised for EMC, but a test of the EMC performance has been carried out. The results of the test are shown in chapter 7, page 48. The test is done with the Y-U-V feature board of the LTI (crosses) and without Y-U-V features (dotted points). The only measure which has been taken before the test, was an extra filter in the vertical outputs (two pignoses and a capacitance of 10nF). As can be seen in the test result of the radiated immunity test, it is completely above the limits.
PR32031 is a single layer board with printed wire bridges.

A large ground area is made underneath the TDA8376(A) itself, to obtain a low ohmic and low inductive ground. A good ground connection runs back from the TDA8376(A) to power plug ”SUPPLY”. The vertical deflection stage has a good local supply decoupling to prevent large AC currents from flowing via plug SUPPLY. The ground connection is wide and does not share any tracks with the TDA8376(A) ground, to prevent hum. A star point near the power supply is usually the best solution.

Special attention should be paid to the following items around the TDA8376(A):

- Decoupling capacitors at supply pin 8 should be as close as possible to the IC and directly back to pin 10, to avoid crosstalk via the supply line.
- Give all emitter followers their own local supply decoupling, very close to the transistor.
- Emitter followers or amplifiers for CVBS output at scart must be placed close to the scart connector and grounded properly to the appropriate scart ground pin.
- Avoid cross-talk between the components and/or tracks from internal and external video sources.
- Video, S-VHS, and other high frequency tracks must be separated from each other by ground or other low ohmic tracks, to avoid crosstalk.
- The bandgap decoupling capacitor at pin 5 must be positioned close to the IC and the ground must be fed back with a short (preferably separate) track to ground pin 10.
- The decoupling capacitor at pin 37 should be close to the IC and back to ground pin 42.
- The filter tuning capacitor connected at pin 12 must be positioned close to the IC.
- The ϕ1 and ϕ2 filters (pins 44 and 43) must be connected close to the IC, with short ground tracks.
- The resistor for the reference current (for geometry part) at pin 52 must be connected close to the IC to a clean ground, just like the vertical sawtooth capacitor at pin 51.
- The colour PLL filter (pin 35) and the reference Xtals (pins 33 and 34) with their series capacitors are connected via a separate wire to the main ground under the IC.
- The ground connections on both sides of the IC should be connected directly to each other, preferably to the ground plane underneath the IC.
- If the tracks to pins 46, 47 and 48 are long, small HF decoupling capacitors are recommended at these pins for EMC immunity.

Also the p.c.b layout around the add-on circuits TDA4665 and TDA8395 needs some attention:

- Supply HF decoupling capacitors should be connected short between TDA4665 pins 1 and 3, and between pins 9 and 10.
- Supply decoupling capacitor at TDA8395 pin 3 should be close to the IC.
- Decoupling capacitors at TDA8395 pins 7 and 8 must be positioned as close as possible to the IC and directly connected to ground pin 6.
- The copper tracks connected at TDA8395 pins 1 and 16 should be properly spaced, to avoid cross-talk between the SECAM reference frequency and the CVBS signal.
- A good, clean ground connection between the TDA8376(A) and the combination of TDA4665 and TDA8395 is necessary. This avoids black offset between PAL and SECAM pictures caused by interference on the ground track during the clamp period.

4.2. Alignment procedures.

Before switching on the demonstration board for the first time, please check the presence of all required components and the absence of short circuits.
Then connect the power supplies to plug ”SUPPLY” and measure if all derived voltages are present. Connect the I²C-bus interface and start up the control software (ICP menu). If everything went well, the ICP menu screen should now indicate ”DEVICE OPERATIONAL”. The status registers of the TDA8376(A) will be read and displayed continuously.

4.2.1. Video amplifiers.

1. Apply a signal with a black picture to the TV receiver.
2. Set brightness and contrast to mid position.
3. Set ”gain” controls WPR, WPG and WPB to mid position (20_{HEX}).
4. Adjust Vg2 voltage to make the black level on the R, G and B cathodes equal to the specified cut-off voltage of the tube. This is done by looking at the highest black current measuring pulse at one of the cathodes at the beginning of the scan (oscilloscope triggered on vertical). This pulse should be 10 V below the desired cut-off voltage of the tube. For detailed information about black current stabilisation, see ref.[7].
5. Apply a signal with a white picture to the TV set. Set contrast control to mid position.
6. Use a colour analyzer to adjust WPR, WPG, WPB to the correct white point colour temperature.
7. Check grey scale.
8. Adjust the focus voltage for a sharp picture on the screen, with high beam-current.

4.2.2. Geometry.

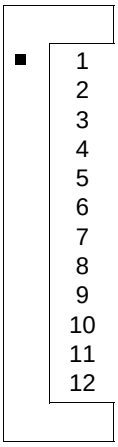
1. Apply a picture with a test circle to the receiver.
2. Adjust brightness and contrast for a normal picture.
3. Use the ICP menu to switch the ”service blanking” on (bottom half blanked).
4. Set the vertical zoom to normal.
5. Adjust the vertical slope ”VSL” until the middle line of the test circle is half visible.
6. Put service blanking off.
7. Adjust the picture height ”VAM”, vertical shift ”VSH” and s-correction ”SC” to the correct values.
8. Adjust the E-W parabola width ”PW” and corner correction ”CP” for perfect straight vertical lines.
9. Adjust the E-W picture width ”EW” and horizontal phase ”HSH”.
10. Adjust the E-W trapezium correction ”TC”.

4.3. Connector description.

The pinning of the connectors on PR32031, -01 and -02 are given below:

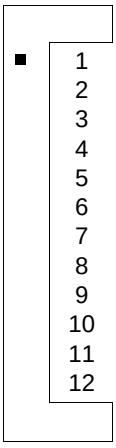
- PR32031 Small signal board for TDA8376(A).
- PR32031-01 Monitor output of RGB and CVBS via Scart connector.
- PR32031-02 H-flyback simulator.

X8 Supply



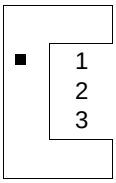
1	Ground
2	+30V
3	+45V
4	+16V
5	+5Vstb
6	Ground
7	+16V
8	+12V
9	+8V
10	+5V
11	Ground
12	n.c.

X9, X18 HOR



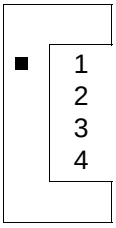
1	Beam Curr. Info
2	Ground
3	H-flyback
4	Ground
5	H-drive
6	Ground
7	EHT-comp.
8	+8V
9	E-W drive
10	Ground
11	ϕ2-comp
12	n.c.

X11 Frontend



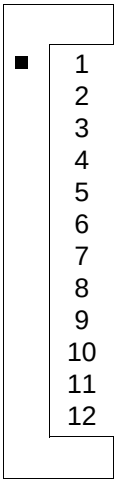
1	n.c.
2	CVBS
3	Ground

X7 I²C



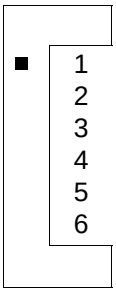
1	SCL
2	Ground
3	+5V
4	SDA

X5 YUV



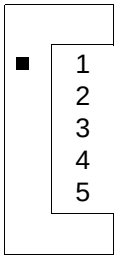
1	R-Y return
2	B-Y return
3	Ground
4	B-Y send
5	R-Y send
6	Reserve
7	Sand
8	SDA
9	SCL
10	+8V
11	Y return
12	Y send

X10 RGBin



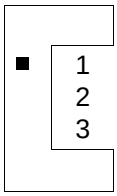
1	CVBS-txt
2	Ground
3	R-in
4	G-in
5	B-in
6	Fblank

X4 CRT



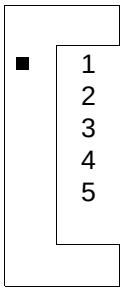
1	I black
2	Ground
3	R out
4	G out
5	B out

X12 Sync



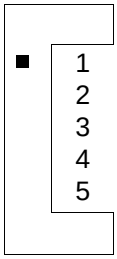
1	Vsync
2	Hsync
3	Ground

X13,X17



1	n.c.
2	+12V
3	ground
4	CVBS-txt
5	ground
	Sandcastle

X14 VERT



1	Coil A
2	Coil A
3	n.c.
4	Coil B
5	Coil B

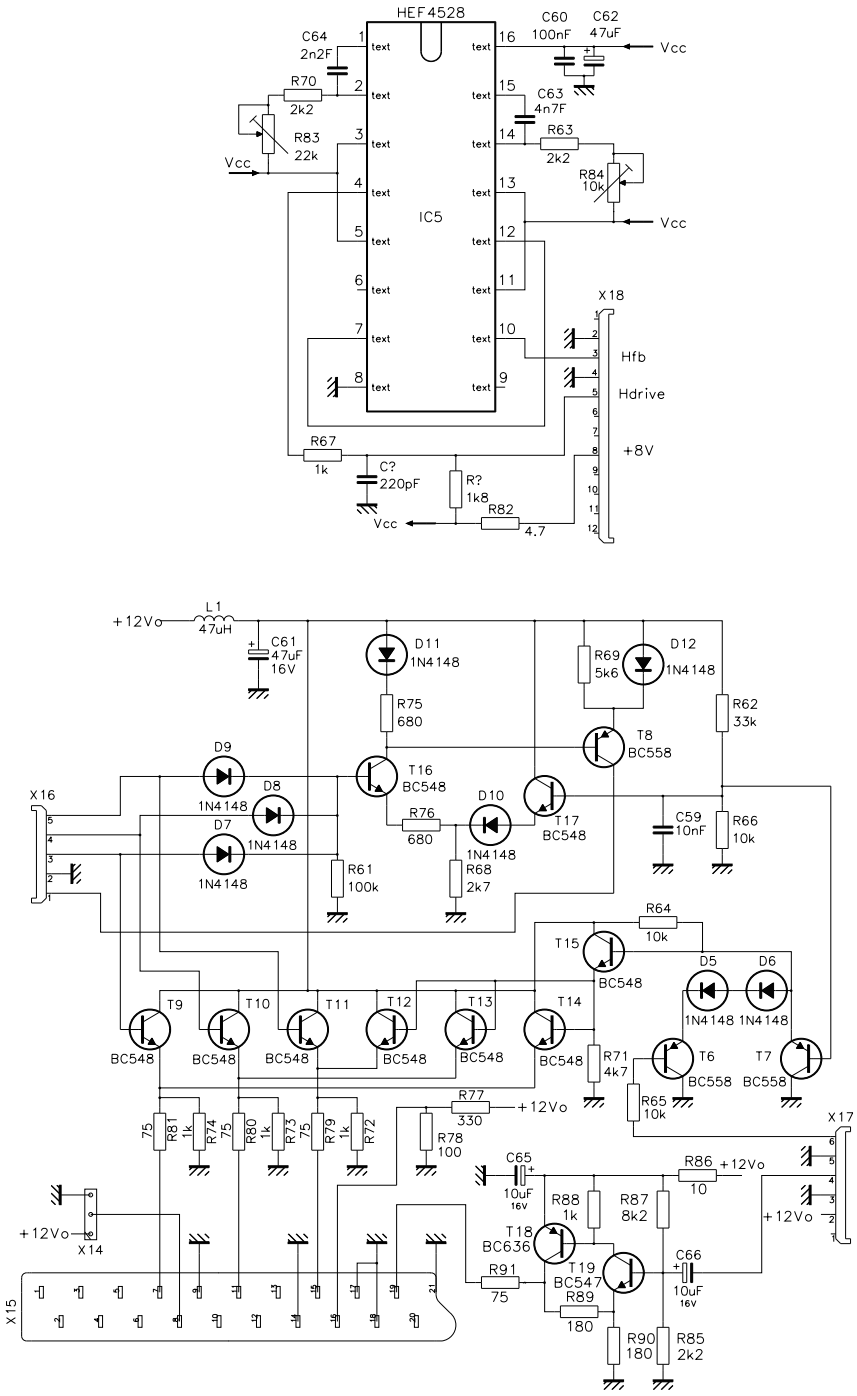


Figure 11 H-flyback simulator and monitor panels.

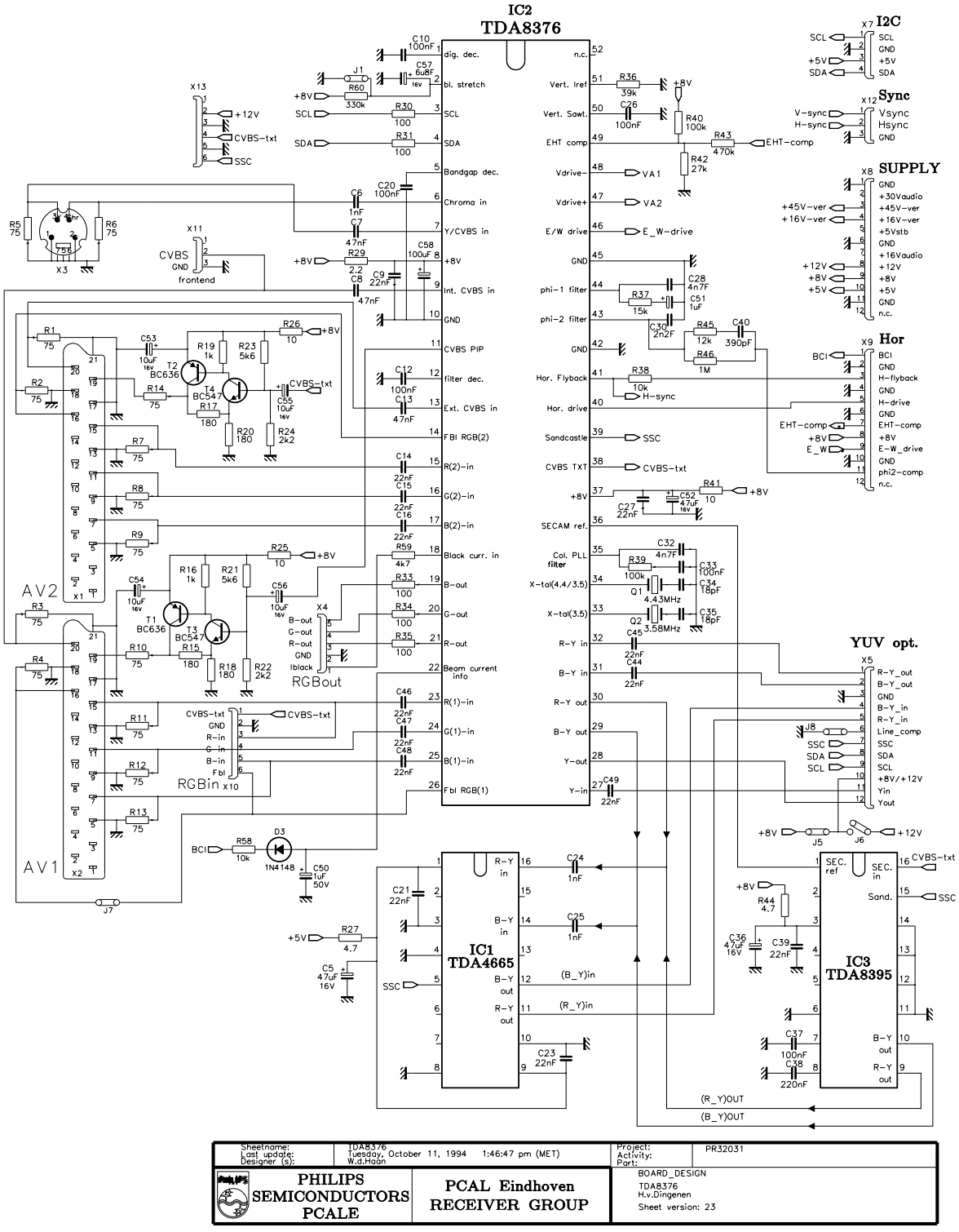


Figure 12 Circuit diagram of TDA8376(A) demonstration board PR32031.

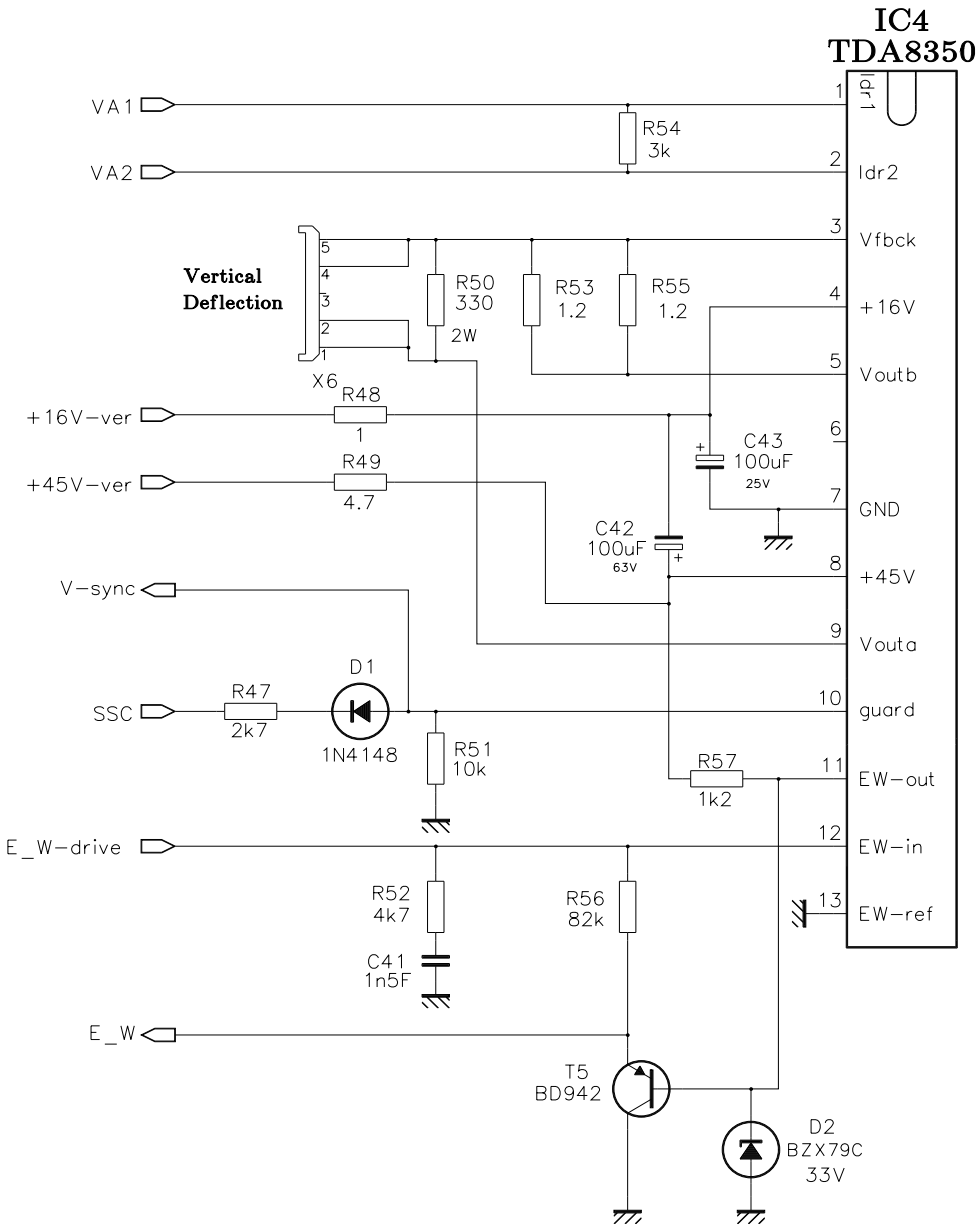


Figure 13 Vertical deflection circuit of the PR32031 board.

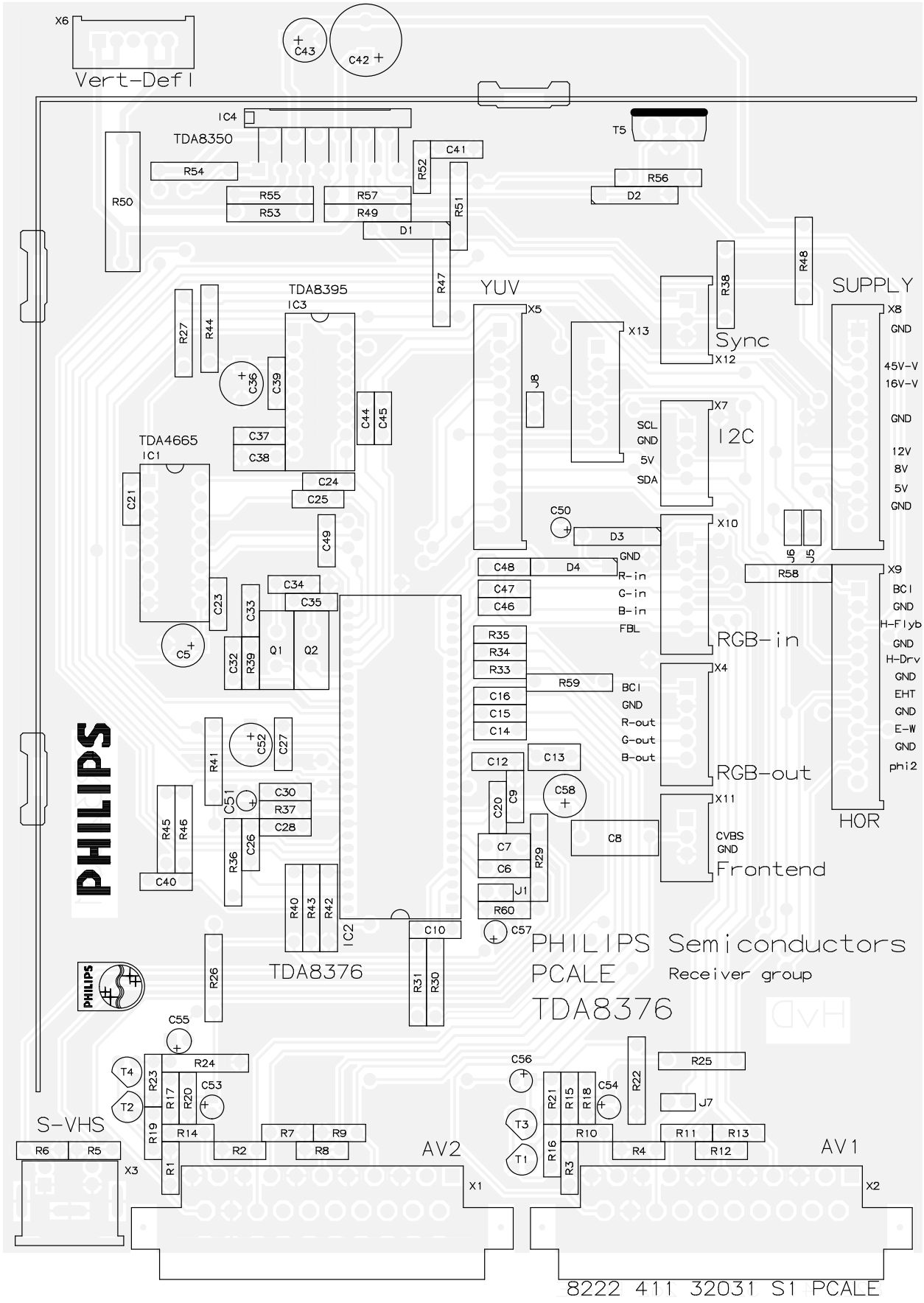


Figure 14 Component positioning and layout of PR32031 board.

5. Bill of materials.

REF	PART NO.	VAL/TYPE	GEOM	SERIES	RATING	TOL.
C5	2222-134-55479	47uF	e_63_2e	C134	16V	20%
C6	2222-629-03102	1nF	cc_36_2e	C629	63V	-20/+80%
C7	2222-370-21473	47nF	fc72_35_2e	C370	100V	10%
C8	2222-368-45473	47nF	fc125_40_4e	C368	250V	10%
C9	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C10	2222-370-11104	100nF	fc72_25_2e	C370	63V	10%
C12	2222-370-11104	100nF	fc72_25_2e	C370	63V	10%
C13	2222-370-21473	47nF	fc72_35_2e	C370	100V	10%
C14	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C15	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C16	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C20	2222-370-11104	100nF	fc72_25_2e	C370	63V	10%
C21	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C23	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C24	2222-629-03102	1nF	cc_36_2e	C629	63V	-20/+80%
C25	2222-629-03102	1nF	cc_36_2e	C629	63V	-20/+80%
C26	2222-370-11104	100nF	fc72_25_2e	C370	63V	10%
C27	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C28	2222-630-03472	4n7F	cc_62_2e	C630	100V	10%
C30	2222-630-03222	2n2F	cc_51_2e	C630	100V	10%
C32	2222-630-03472	4n7F	cc_62_2e	C630	100V	10%
C33	2222-370-11104	100nF	fc72_25_2e	C370	63V	10%
C34	2222-631-10189	18pF	cc_36_2e	C631-NP0	100V	
C35	2222-631-10189	18pF	cc_36_2e	C631-NP0	100V	
C36	2222-134-55479	47uF	e_63_2e	C134	16V	20%
C37	2222-370-11104	100nF	fc72_25_2e	C370	63V	10%
C38	2222-370-11224	220nF	fc72_35_2e	C370	63V	10%
C39	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C40	2222-630-03391	390pF	cc_36_2e	C630	100V	10%
C41	2222-630-03152	1n5F	cc_45_2e	C630	100V	10%
C42	2222-037-68101	100uF	e_105_2e	C037	63V	20%
C43	2222-037-90047	100uF	e_65_2e	C037	25V	20%
C44	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C45	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C46	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C47	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C48	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C49	2222-629-03223	22nF	cc_62_2e	C629	63V	-20/+80%
C50	2222-134-61108	1uF	e_30_1e	C134	50V	20%
C51	2222-134-61108	1uF	e_30_1e	C134	50V	20%
C52	2222-134-55479	47uF	e_63_2e	C134	16V	20%
C53	2222-134-65109	10uF	e_35_1e	C134	16V	20%
C54	2222-134-65109	10uF	e_35_1e	C134	16V	20%
C55	2222-134-65109	10uF	e_35_1e	C134	16V	20%
C56	2222-134-65109	10uF	e_35_1e	C134	16V	20%
C57	2222-134-65688	6u8F	e_35_1e	C134	16V	20%
C58	2222-037-90047	100uF	e_65_2e	C037	25V	20%
C59	2222-629-03103	10nF	cc_45_2e	C629	63V	-20/+80%
C60	2222-370-11104	100nF	fc72_25_2e	C370	63V	10%
C61	2222-134-55479	47uF	e_63_2e	C134	16V	20%
C62	2222-134-55479	47uF	e_63_2e	C134	16V	20%
C63	2222-630-03472	4n7F	cc_51_2e	C630	100V	10%
C64	2222-630-03222	2n2F	cc_62_2e	C630	100V	10%

REF	PART NO.	VAL/TYPE	GEOM	SERIES	RATING	TOL.
C65	2222-134-65109	10uF	e_35_1e	C134	16V	20%
C66	2222-134-65109	10uF	e_35_1e	C134	16V	20%
D1	9330-839-90153	1N4148	do_35			
D2	9331-179-10153	33V	do_35	BZX79C		
D3	9330-839-90153	1N4148	do_35			
D4	9330-839-90153	1N4148	do_35			
D5	9330-839-90153	1N4148	do_35			
D6	9330-839-90153	1N4148	do_35			
D7	9330-839-90153	1N4148	do_35			
D8	9330-839-90153	1N4148	do_35			
D9	9330-839-90153	1N4148	do_35			
D10	9330-839-90153	1N4148	do_35			
D11	9330-839-90153	1N4148	do_35			
D12	9330-839-90153	1N4148	do_35			
IC1	PN-TDA4665	TDA4665	dil16			
IC2	PN-TDA8376(A)	TDA8376(A)	sr_dil52			
IC3	PN-TDA8395	TDA8395	dil16			
IC4	PN-TDA8350	TDA8350	qsil13			
IC5	PN-hef4528	hef4528	dil16			
J1	PN-JUMPER-1x2p	jumper_2p	jumper_1x2p			
J5	PN-JUMPER-1x2p	jumper_2p	jumper_1x2p			
J6	PN-JUMPER-1x2p	jumper_2p	jumper_1x2p			
J7	PN-JUMPER-1x2p	jumper_2p	jumper_1x2p			
J8	PN-JUMPER-1x2p	jumper_2p	jumper_1x2p			
L1	LAL02TB_470K	47uH	uchoke_2e	UCHOKE	10%	
Q1	PN-XTAL-4.43MHz	4.43MHz	rw43	SERIES		
Q2	PN-XTAL-3.58MHz	3.58MHz	rw43	SERIES		
R1	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R2	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R3	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R4	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R5	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R6	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R7	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R8	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R9	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R10	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R11	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R12	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R13	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R14	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R15	2322-180-73181	180	r_19_2e	SFR16T	0.5W	5%
R16	2322-180-73102	1K	r_19_2e	SFR16T	0.5W	5%
R17	2322-180-73181	180	r_19_2e	SFR16T	0.5W	5%
R18	2322-180-73181	180	r_19_2e	SFR16T	0.5W	5%
R19	2322-180-73102	1K	r_19_2e	SFR16T	0.5W	5%
R20	2322-180-73181	180	r_19_2e	SFR16T	0.5W	5%
R21	2322-180-73562	5K6	r_19_2e	SFR16T	0.5W	5%
R22	2322-186-16222	2K2	r_25_4e	SFR25H	0.5W	5%
R23	2322-180-73562	5K6	r_19_2e	SFR16T	0.5W	5%
R24	2322-186-16222	2K2	r_25_4e	SFR25H	0.5W	5%
R25	2322-186-16109	10	r_25_4e	SFR25H	0.5W	5%
R26	2322-186-16109	10	r_25_4e	SFR25H	0.5W	5%
R27	2322-207-13478	4.7	r_25_4e	NFR25H	0.5W	5%
R29	2322-207-13228	2.2	r_25_4e	NFR25H	0.5W	5%

REF	PART NO.	VAL/TYPE	GEOM	SERIES	RATING	TOL.
R30	2322-186-16101	100	r_25_4e	SFR25H	0.5W	5%
R31	2322-186-16101	100	r_25_4e	SFR25H	0.5W	5%
R33	2322-180-73101	100	r_19_2e	SFR16T	0.5W	5%
R34	2322-180-73101	100	r_19_2e	SFR16T	0.5W	5%
R35	2322-180-73101	100	r_19_2e	SFR16T	0.5W	5%
R36	2322-186-16393	39K	r_25_4e	SFR25H	0.5W	5%
R37	2322-180-73153	15K	r_19_2e	SFR16T	0.5W	5%
R38	2322-186-16103	10K	r_25_4e	SFR25H	0.5W	5%
R39	2322-180-73104	100K	r_19_2e	SFR16T	0.5W	5%
R40	2322-186-16104	100K	r_25_4e	SFR25H	0.5W	5%
R41	2322-207-13109	10	r_25_4e	NFR25H	0.5W	5%
R42	2322-186-16273	27K	r_25_4e	SFR25H	0.5W	5%
R43	2322-186-16474	470K	r_25_4e	SFR25H	0.5W	5%
R44	2322-207-13478	4.7	r_25_4e	NFR25H	0.5W	5%
R45	2322-186-16123	12K	r_25_4e	SFR25H	0.5W	5%
R46	2322-186-16105	1M	r_25_4e	SFR25H	0.5W	5%
R47	2322-186-16272	2K7	r_25_4e	SFR25H	0.5W	5%
R48	2322-207-13108	1	r_25_4e	NFR25H	0.5W	5%
R49	2322-207-13478	4.7	r_25_4e	NFR25H	0.5W	5%
R50	2322-194-13331	330	pr02_7e	PR02	2W	5%
R51	2322-186-16103	10K	r_25_4e	SFR25H	0.5W	5%
R52	2322-180-73472	4K7	r_19_2e	SFR16T	0.5W	5%
R53	2322-186-16128	1.2	r_25_4e	SFR25H	0.5W	5%
R54	2322-186-16302	3K	r_25_4e	SFR25H	0.5W	5%
R55	2322-186-16128	1.2	r_25_4e	SFR25H	0.5W	5%
R56	2322-186-16823	82K	r_25_4e	SFR25H	0.5W	5%
R57	2322-186-16122	1K2	r_25_4e	SFR25H	0.5W	5%
R58	2322-186-16103	10K	r_25_4e	SFR25H	0.5W	5%
R59	2322-186-16472	4K7	r_25_4e	SFR25H	0.5W	5%
R60	2322-180-73334	330K	r_19_2e	SFR16T	0.5W	5%
R61	2322-180-73104	100K	r_19_2e	SFR16T	0.5W	5%
R62	2322-180-73333	33K	r_19_2e	SFR16T	0.5W	5%
R63	2322-180-73562	5K6	r_19_2e	SFR16T	0.5W	5%
R64	2322-180-73103	10K	r_19_2e	SFR16T	0.5W	5%
R65	2322-180-73103	10K	r_19_2e	SFR16T	0.5W	5%
R66	2322-180-73103	10K	r_19_2e	SFR16T	0.5W	5%
R67	2322-180-73103	10K	r_19_2e	SFR16T	0.5W	5%
R68	2322-180-73272	2k7	r_19_2e	SFR16T	0.5W	5%
R69	2322-180-73562	5K6	r_19_2e	SFR16T	0.5W	5%
R70	2322-180-73223	22K	r_19_2e	SFR16T	0.5W	5%
R71	2322-180-73472	4K7	r_19_2e	SFR16T	0.5W	5%
R72	2322-180-73102	1K	r_19_2e	SFR16T	0.5W	5%
R73	2322-180-73102	1K	r_19_2e	SFR16T	0.5W	5%
R74	2322-180-73102	1K	r_19_2e	SFR16T	0.5W	5%
R75	2322-180-73681	680	r_19_2e	SFR16T	0.5W	5%
R76	2322-180-73681	680	r_19_2e	SFR16T	0.5W	5%
R77	2322-180-73331	330	r_19_2e	SFR16T	0.5W	5%
R78	2322-180-73101	100	r_19_2e	SFR16T	0.5W	5%
R79	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R80	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R81	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
R82	2322-205-13478	4.7	r_25_4e	NFR25	0.33W	5%
R83	2322-482-30223	22K	omp10_v	OMP10	0.5W	20%
R84	2322-482-30103	10K	omp10_v	OMP10	0.5W	20%
R85	2322-186-16222	2K2	r_25_4e	SFR25H	0.5W	5%

REF	PART NO.	VAL/TYPE	GEOM	SERIES	RATING	TOL.
R86	2322-186-16109	10	r_25_4e	SFR25H	0.5W	5%
R87	2322-180-73822	8K2	r_19_2e	SFR16T	0.5W	5%
R88	2322-180-73102	1K	r_19_2e	SFR16T	0.5W	5%
R89	2322-180-73181	180	r_19_2e	SFR16T	0.5W	5%
R90	2322-180-73181	180	r_19_2e	SFR16T	0.5W	5%
R91	2322-180-73759	75	r_19_2e	SFR16T	0.5W	5%
T1	9332-219-50112	BC636	to_92			
T2	9332-219-50112	BC636	to_92			
T3	9331-976-10112	BC547	to_92			
T4	9331-976-10112	BC547	to_92			
T5	PN-BD942	BD942	to_220			
T6	9331-977-30116	BC558	to_92			
T7	9331-977-30116	BC558	to_92			
T8	9331-977-30116	BC558	to_92			
T9	9331-976-40112	BC548	to_92			
T10	9331-976-40112	BC548	to_92			
T11	9331-976-40112	BC548	to_92			
T12	9331-976-40112	BC548	to_92			
T13	9331-976-40112	BC548	to_92			
T14	9331-976-40112	BC548	to_92			
T15	9331-976-40112	BC548	to_92			
T16	9331-976-40112	BC548	to_92			
T17	9331-976-40112	BC548	to_92			
T18	9332-219-50112	BC636	to_92			
T19	9331-976-10112	BC547	to_92			
X1	TEXIM-VP-1CH	EURO_SCART	euro_scart			
X2	TEXIM-VP-1CH	EURO_SCART	euro_scart			
X3	s-vhs	svhs_5p	svhs			
X4	MKS3735-1-0-505	MKS3730_5p	mks3730_5p			
X5	MKS3742-1-0-1212	MKS3730_12p	mks3730_12p			
X6	MKS3735-1-0-505	MKS3730_5p	mks3730_5p			
X7	MKS3734-1-0-404	MKS3730_4p	mks3730_4p			
X8	MKS3742-1-0-1212	MKS3730_12p	mks3730_12p			
X9	MKS3742-1-0-1212	MKS3730_12p	mks3730_12p			
X10	MKS3736-1-0-606	MKS3730_6p	mks3730_6p			
X11	MKS3733-1-0-303	MKS3730_3p	mks3730_3p			
X12	MKS3733-1-0-303	MKS3730_3p	mks3730_3p			
X13	MKS3736-1-0-606	MKS3730_6p	mks3730_6p			
X14	2422-024-04008	ARRAY_1x3p	array_1x3p			
X15	TEXIM-VP-1CH	EURO_SCART	euro_scart			
X16	MKS3735-1-0-505	MKS3730_5p	mks3730_5p			
X17	MKS3736-1-0-606	MKS3730_6p	mks3730_6p			
X18	MKF1512-1-0-1212	MKF1500_12p	mkf1500_12p			

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7. EMC test result.